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VOLTAGE STRESS EFFECTS ON MICROCIRCUIT ACCELERATED LIFE TEST FAILURE RATES

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MCDONNELL DOUGLAS ASTRONAUTICS COMPANY - EAST

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The applicability of Arrhenius and Eyring reaction rate models for describing microcircuit aging characteristics as a function of junction temperature and applied voltage was evaluated. The results of a matrix of accelerated life tests with a single CMOS microcircuit type operated at six different combinations of temperature and voltage were used to evaluate the models. A total of 450 devices from two different lots were tested at ambient temperatures between 200°C and 250°C and applied voltages between 5 Vdc and 15 Vdc. Initially only a single lot of

20. ABSTRACT (Continued)

devices (Lot A) was included in the program. However, this particular lot of devices experienced excessive package related failures due to thermal cycling effects during accelerated life testing. As a result of these package related problems, a second lot of devices in a different package (Lot B) was included in the program. Analysis of the 286 total failed devices in Lot A and Lot B indicated that 42.3% were due to Lot A package defects, 11.5% were due to wire-to-die shorts, and 39.2% were due to surface related defects. The remaining failures (7%) were due to bulk silicon and other defects. Statistical analysis of the surface related failure data resulted in bimodal failure distributions comprised of two lognormal distributions; a "freak" distribution observed early in time, and a "main" distribution observed later in time. The Arrhenius model was shown to provide a good description of device aging as a function of temperature at a fixed voltage. The Eyring model also appeared to provide a reasonable description of main distribution device aging as a function of temperature and voltage. However, there was insufficient failure data from the life tests to permit a rigorous evaluation of the Eyring model for the "main" distribution. In addition, the "freak" distribution of device lifetimes did not appear to be a function of applied voltage. Since the "freak" distribution failures were due to cation drift in gate oxides, the lack of voltage dependence was not expected. However, almost all of the "freak" failures occurred in less than one (1) hour at the accelerated test temperatures which hampered an accurate determination of actual failure times. Further studies at test temperatures below 200°C may yield more accurate failure times and provide better visibility of voltage effects that may exist.

PREFACE

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company-East (MDAC-EAST) Engineering Reliability Department during the period between September 1974 and July 1976. The work was performed for the National Aeronautics and Space Administration (NASA), George C. Marshall Space Flight Center under Contract Number NAS8-31177. Mr. W. R. Barlow acted as the NASA Contracting Officer's Representative. Significant technical contributions were made by Messrs. Morton Stitch, Bruce Kirk, Roy Maurer and Ed Sisul of the MDAC-EAST Engineering Reliability Department.

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1.0 INTRODUCTION

Extensive accelerated test studies of microcircuits using both temperature and voltage as failure accelerating stresses have been performed by McDonnell Douglas, Bell Telephone Laboratories and the British Post Office Research Center [1, 2, 3]. All of these studies have shown the applicability of an Arrhenius reaction rate model [4] for describing semiconductor aging characteristics as a function of temperature. However, the effects of applied voltage upon the observed aging characteristics have not been fully explored. Prior work at McDonnell Douglas sponsored by the Rome Air Development Center (Contract No. F30602-73-C-0140) included accelerated life tests at several different voltage conditions. The results of the MDAC-EAST studies indicated that electrical bias voltage was necessary to accelerate surface related failures in a reasonable time period, and that device operation at reduced voltage generally resulted in an increased median lifetime for the test population. Evaluation of the test results suggested the applicability of an Eyring reaction rate model [4], which includes both temperature and a nonthermal stress factor, to describe microcircuit aging characteristics. Unfortunately, the number of different temperature/voltage combinations at which life test data had been generated was not sufficient for a rigorous evaluation of an Eyring model.

The accelerated test program described in this report was designed to provide sufficient life test data to evaluate both the Arrhenius and Eyring models. Life tests were conducted at six different combinations of temperature and applied voltage. Two lots of a single manufacturer's Complementary Metal Oxide Semiconductor (CMOS) device were tested at ambient temperatures between 200°C and 250°C and applied voltages between 5 Vdc and 15 Vdc. The results of these tests are discussed in terms of the observed failure modes/mechanisms, failure distributions and the applicability of Arrhenius and Eyring reaction rate models for describing device aging characteristics.

2.0 PROGRAM DESCRIPTION

The program for evaluating the effects of voltage stress on microcircuit failure rates was accomplished in accordance with the work flow illustrated in Figure 1. Initially a single lot of one manufacturer's CMOS 4007 (Dual Complementary Pair plus Inverter) devices (Lot A) was included in the program. However, this particular lot of devices experienced excessive package related failures due to thermal cycling effects during accelerated life testing. As a result of these package related problems, a second lot of CMOS 4007 devices in a different package (Lot B) was included in the program. Both lots of devices were procured to the MIL-M-38510 Class C processing requirements plus 100% electrical testing at -55°C and 125°C.

Upon receipt of devices, electrical tests were performed to characterize device performance at 25°C and to provide the zero hour baseline data for the subsequent accelerated life tests. A sample of each lot of devices was also subjected to a destructive physical analysis to characterize construction features, and to evaluate physical characteristics of the device that could impact the life test results. Due to the Lot A package problems, special Lot B package integrity tests were also performed with a sample of the Lot B devices. These tests consisted of a sequence of: a) seal leak tests, b) thermal shock tests, c) seal leak tests, and d) visual examinations.

Concurrent with the Lot A device characterization activities, studies were performed to select suitable nondestructive accelerated life test conditions. Candidate bias circuits for the accelerated life tests were evaluated at ambient temperatures between 200°C and 285°C to select a biasing configuration that maintained maximum voltage across the device at a controlled low value of current. Device thermal characteristics were then examined while operating a device in the selected bias circuit at ambient temperatures between 200°C and 250°C. Both electrical and infrared mapping techniques were employed to determine maximum junction temperatures and thermal gradients across the chip surface. As a final check of the suitability of the high temperature bias circuit, and to aid in the selection of specific accelerated test temperatures, a step-stress test was performed with 20 Lot A devices.

FIGURE 1. PROGRAM WORK FLOW

Upon completion of the step stress test, nondestructive ambient test temperatures of 200°C, 225°C and 250°C were selected for life testing. Bias voltages of 5 Vdc, 10 Vdc and 15 Vdc were also selected. The temperature-voltage combinations are as shown in the previously mentioned Figure 1. Forty Lot A, and thirty-five Lot B devices were operated at each of the six temperature/voltage combinations. Each life test was conducted for 4,000 hours or 50% failure, whichever occurred first. The basic test sequence used during life testing is shown in Figure 2. The initial, interim and final electrical tests are identical, and consisted of the MIL-M-38510 Group A dc parameter tests at 25°C. Details of the electrical test conditions and end-point limits are contained in Appendix A. However, it should be noted that the test conditions and end-point limits were not identical for Lot A and Lot B devices. Lot A devices were tested to the MIL-M-38510/053 (NASA) specification requirements, and Lot B devices were tested to the MIL-M-38510/053A specification requirements. In addition, some of the MIL-M-38510 electrical specification limits were relaxed to permit procurement of devices. Interim electrical measurements were performed, after allowing the devices to cool to room temperature with bias applied, at the following times: 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1,000, 2,000, 3,000 and 4,000 hours. A control sample (five devices stored at room ambient conditions) was also tested each time electrical measurements were performed. The purpose of the control sample was to provide a check on the stability of the automated test equipment used for electrical testing. All devices that failed an interim electrical test were subjected to a detailed failure analysis to determine the failure mode, mechanism and most probable cause of failure.

At the completion of the life test matrix, the data was statistically analyzed to determine the nature of the failure distribution at each temperature/voltage combination. Median life-times from each failure distribution were then used to evaluate the applicability of the Arrhenius and Eyring reaction rate models for describing microcircuit aging characteristics.

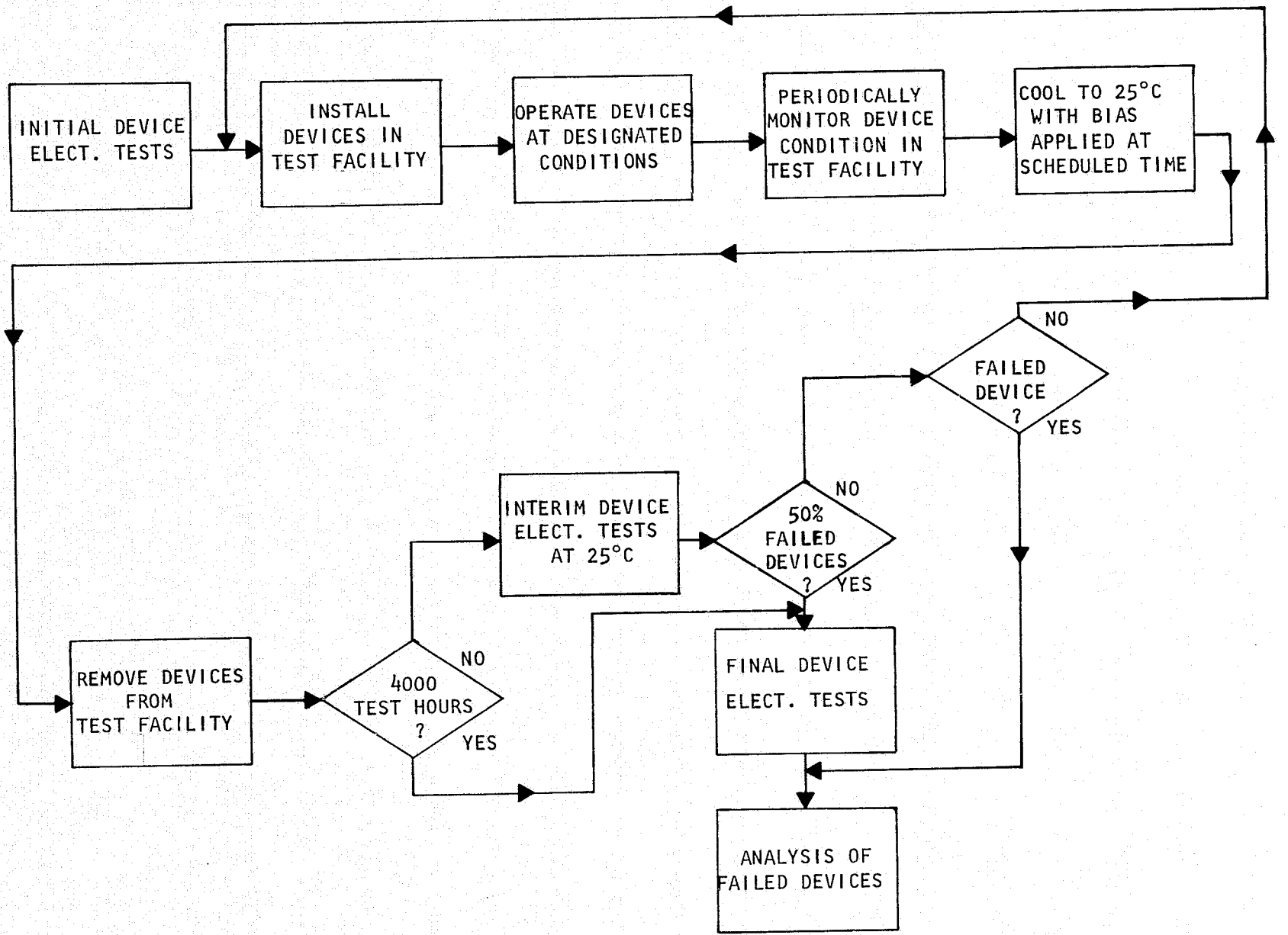


FIGURE 2. LIFE TESTING SEQUENCE

3.0 TEST VEHICLE

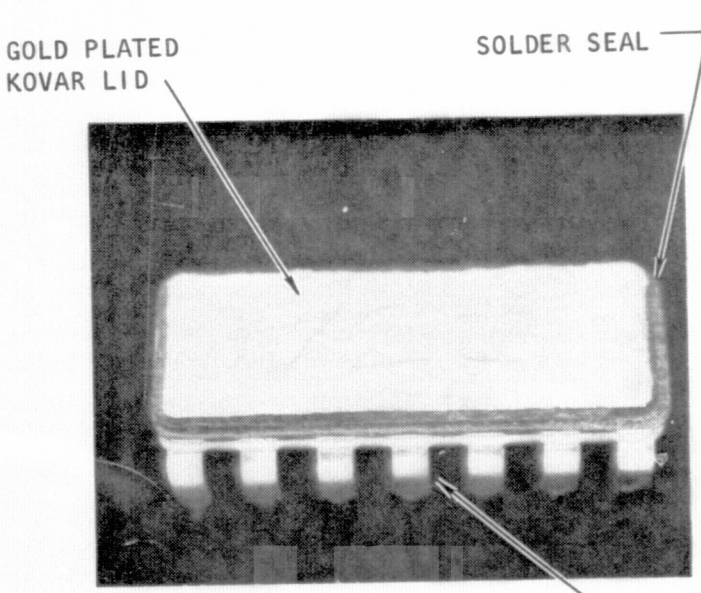
A CMOS device was selected to evaluate voltage stress effects on microcircuit life characteristics since MOS devices are susceptible to voltage dependent surface effect failure mechanisms such as ion drift in gate oxides. The 4007, Dual Complementary Pair plus Inverter, was selected as the particular device type for flexibility of life test bias circuit design and ease of failure analysis.

Both Lot A and Lot B devices were provided in 14 pin dual-in-line ceramic packages with gold plated leads. Pertinent physical features of Lot A devices are summarized in Figure 3. Detailed optical and SEM examinations of the devices, as documented in Appendix B, did not reveal any construction features or physical anomalies that would adversely affect the life test results. However, as later discovered, Lot A ceramic packages were unable to withstand the repeated temperature cycling experienced during life testing at the times electrical measurements are performed. The Lot B replacement devices were identical to the Lot A devices except for the package construction. The differences in package construction details are illustrated in Figure 4. Note that the external leads of Lot A devices are integral with the internal lead frame, whereas the Lot B devices have external leads that are brazed to the internal lead frame. Since the Lot A package failures were due to cracks in the ceramic as a result of thermal expansion and contractions of the lead frame, a sample of Lot B devices was subjected to thermal shock package integrity tests prior to life testing. Fifteen (15) Lot B devices were subjected to twenty (20) liquid-to-liquid thermal shocks from -50°C to 175°C in accordance with MIL-STD-883 Method 1011.1. None of the devices exhibited loss of hermeticity or visual evidence of damage after the thermal shock test. Construction details of the Lot B devices are contained in Appendix B.

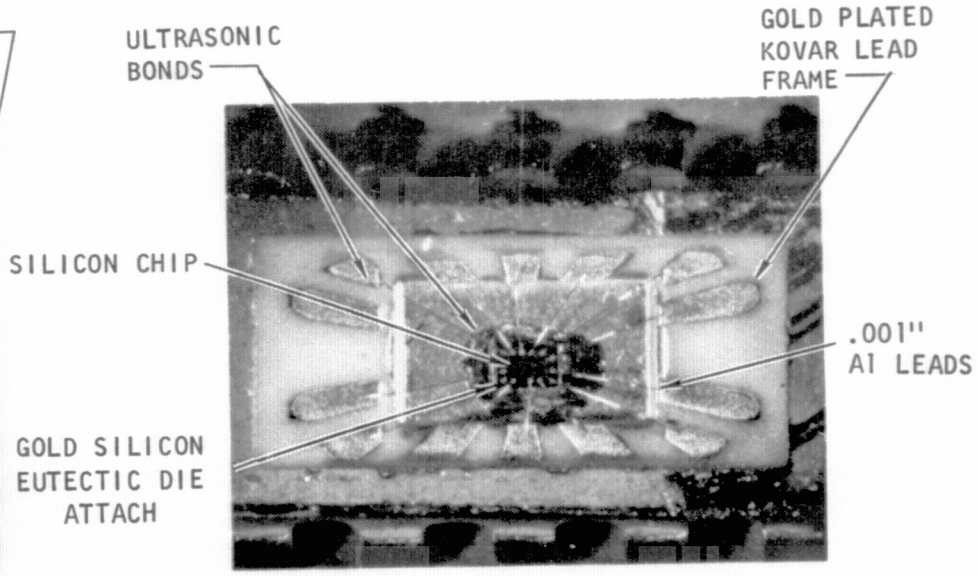
Initial electrical parameter tests performed at 25°C with all Lot A and Lot B devices resulted in the parameter characterizations shown in Tables 1 and 2. Test conditions used for electrical testing are contained in Appendix A, and are, as previously mentioned, the MIL-M-38510/053 (NASA) and MIL-M-38510/053A conditions. A gate to source threshold voltage test was also performed, but no

failure criteria was established for this parameter. With the following exceptions, parameter limits are MIL-M-38510/053 limits:

Lot A	V_{OH1}	changed from 4.2 Vdc min to 3.6 Vdc min
	I_{IH} & I_{IL}	changed from 1nA max to 10nA max
Lot B	V_{OH2}	changed from 4.5 Vdc min to 4.0 Vdc min
	V_{OL2}	changed from 0.5 Vdc max to 0.6 Vdc max
	I_{IH} & I_{IL}	changed from 3nA max to 10nA max



A. EXTERNAL CONSTRUCTION



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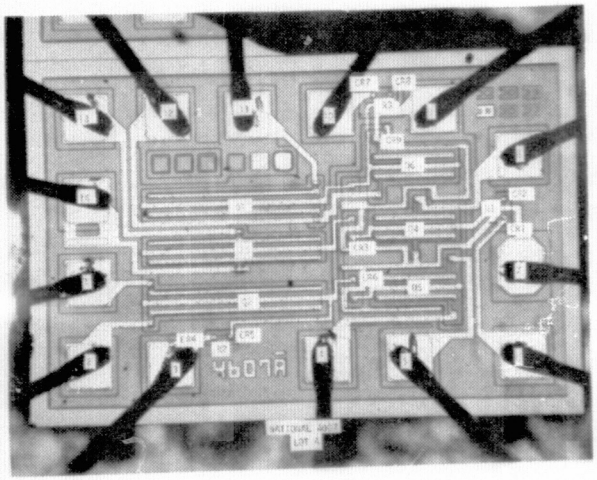

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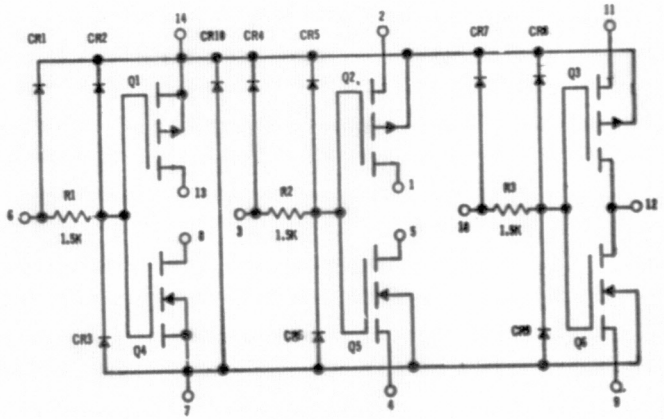
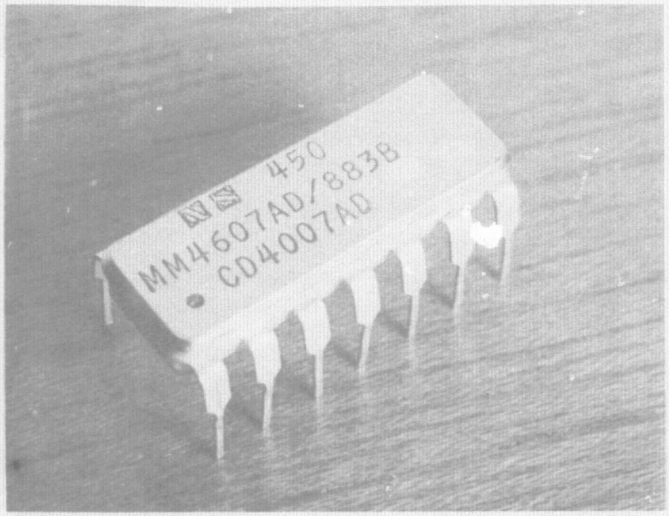
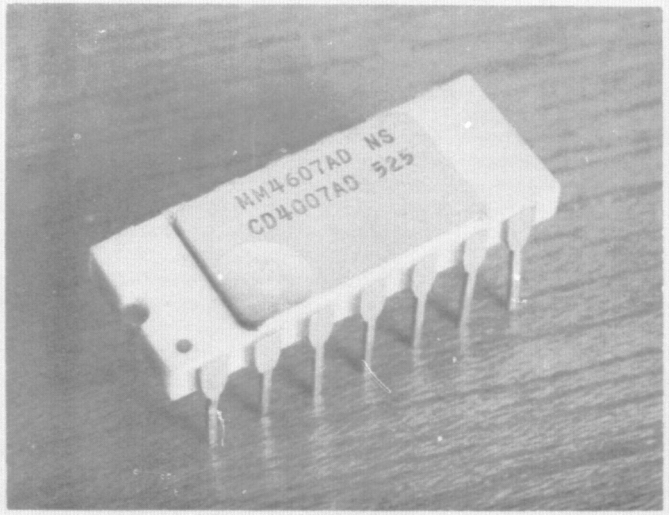
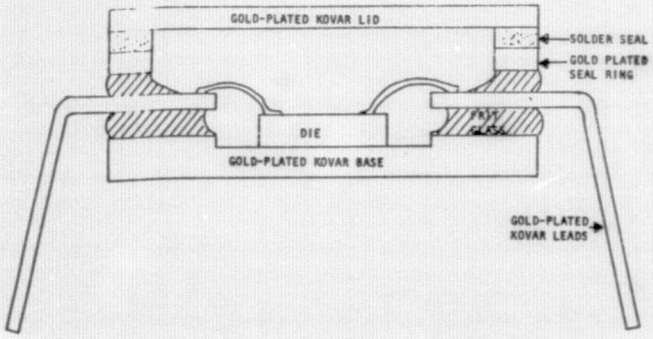


D. FUNCTIONAL SCHEMATIC

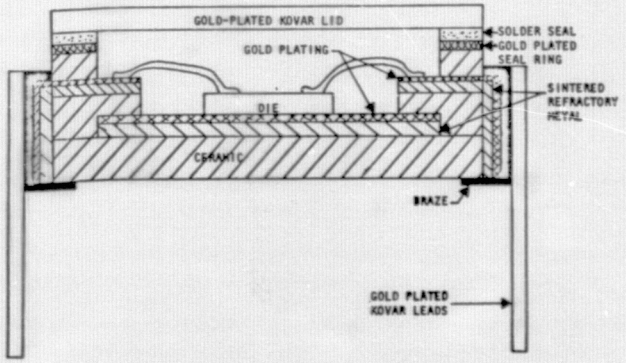
FIGURE 3 . LOT A CONSTRUCTION DETAILS







LOT A



LOT B

FIGURE 4. COMPARISON OF LOT A & LOT B PACKAGE CONSTRUCTION

TABLE 1. 25°C PARAMETER CHARACTERIZATION - LOT A

PARAMETER	LIMITS		MEAN	SIGMA	UNITS
	MIN	MAX			
I_{IL}		-10.0	-0.018	0.109	nA
I_{IH}		10.0	0.029	0.128	nA
V_{OL1}		0.4	0.246	0.009	Vdc
V_{OL2}		10.0	0.022	0.008	mVdc
V_{OH1}	3.6		4.135	0.085	Vdc
V_{OH2}		10.0	-0.016	0.019	mVdc
V_{O3}		10.0	0.018	0.299	mVdc
V_{O6}		0.1	0.000	0.000	Vdc
I_{SSH}		-50.0	-1.117	3.802	nA
I_{SSL}		-50.0	-0.748	0.870	nA
$V_{TH(P)}$	*		1.470	0.096	Vdc
$V_{TH(N)}$	*		1.787	0.057	Vdc

* THESE TESTS ARE NOT MIL-M-38510 TESTS.

TABLE 2. 25°C PARAMETER CHARACTERIZATION - LOT B

PARAMETER	LIMITS		MEAN	SIGMA	UNITS
	MIN	MAX			
$V_{IC(+)}$		1.5	0.847	0.016	Vdc
$V_{IC(-)}$		-6.0	-1.004	0.025	Vdc
I_{SSH}		-50.0	-0.792	2.864	nA
I_{SSL}		-50.0	-1.596	2.903	nA
V_{OH1}	2.5		4.408	0.000	Vdc
V_{OH2}	4.0		4.352	0.068	Vdc
V_{OH3}	4.95		5.000	0.000	Vdc
V_{OH4}	11.25		12.274	0.121	Vdc
V_{OL1}		0.4	0.169	0.019	Vdc
V_{OL2}		0.6	0.434	0.031	Vdc
V_{OL3}		50.0	0.026	0.059	mVdc
V_{OL4}		1.25	0.396	0.083	Vdc
I_{IH1}		10.0	0.416	1.108	nA
I_{IL1}		-10.0	-0.624	1.377	nA
$V_{TH(P)}$	*		1.522	0.086	Vdc
$V_{TH(N)}$	*		1.379	0.118	Vdc

* THESE TESTS ARE NOT MIL-M-38510 TESTS.

4.0 SELECTION OF LIFE TEST CONDITIONS

The selection of bias circuits, test temperatures and test voltages was accomplished in accordance with the sequence shown in Figure 5. Initially, candidate bias circuits were evaluated at ambient temperatures between 200°C and 285°C in an attempt to find a bias circuit that:

(a) maintained maximum rated voltage at the device terminals over the temperature range to provide maximum acceleration of surface effect failure mechanisms,

(b) maintained the device current at a controlled low level to minimize failures due to thermal runaway and electromigration,

(c) maintained a consistent set of internal microcircuit stress (primarily voltage) conditions over the temperature range (A drastic difference between circuit node voltages at different accelerated test temperatures may invalidate subsequent calculations of acceleration factors.), and

(d) provided both positive and negative voltage stress across gate oxides to accelerate both n and p-channel transistor failures due to positive and negative species of charge contamination.

Once a bias circuit satisfied the above objectives, a thermal characterization of the microcircuit was performed with the device operated in the selected bias circuit. Both electrical and infrared scanning techniques were utilized to determine the maximum junction temperature and thermal gradient across the chip surface. Step stress tests were then performed to verify the suitability of the bias circuit and to aid in the selection of accelerated life test temperatures.

4.1 Bias Circuit Evalutions

The selection of a suitable bias circuit for the 4007 microcircuit evolved from a study of the device schematic, and high temperature tests of the most promising candidate circuits. Three candidate bias circuits (A, B and C) were evaluated. All of the candidate circuits configured the device as three inverters with no load on the outputs. Circuit "A" placed all inputs low, Circuit "B" placed all inputs high, and Circuit "C" placed two inputs low and one input high. The results of testing several devices in these circuits at ambient temperatures

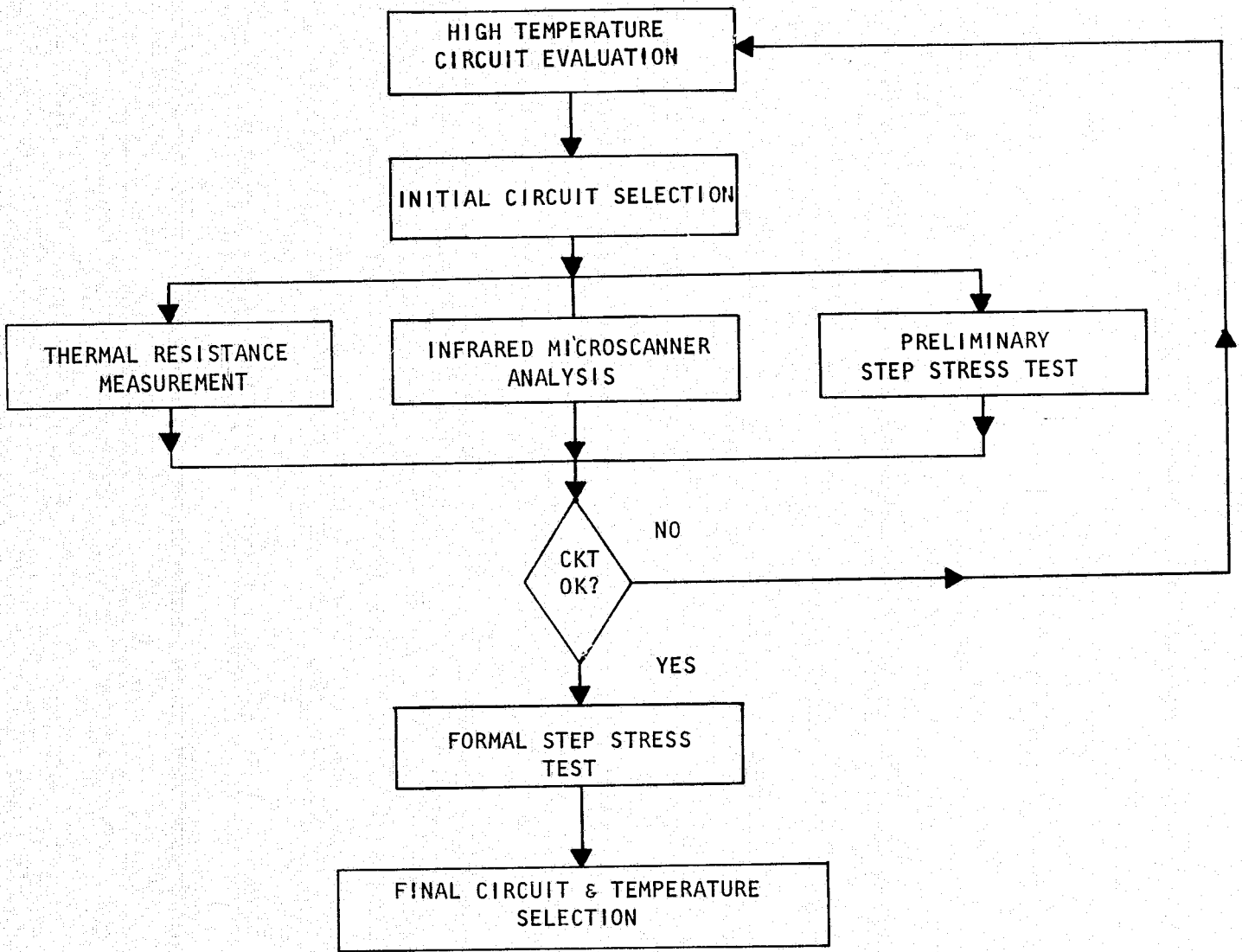


FIGURE 5. TEST SEQUENCE FOR SELECTION OF LIFE TEST CONDITIONS

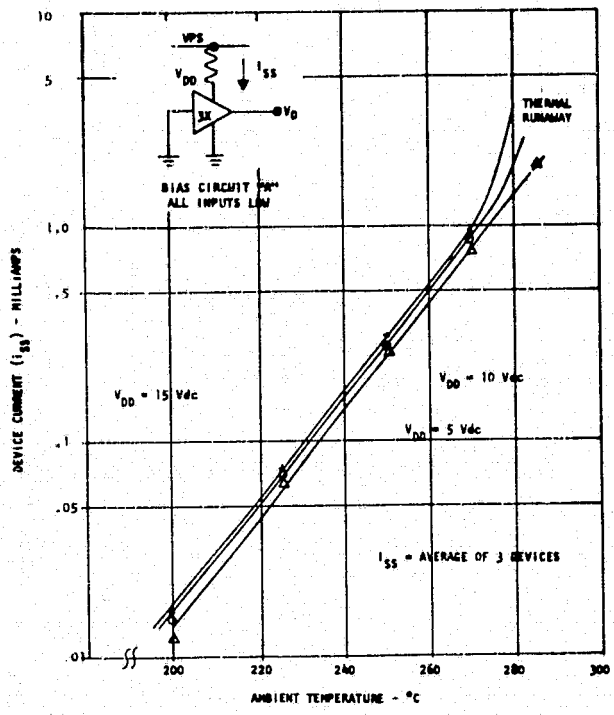
between 200°C and 285°C, and voltages between 5 Vdc and 15 Vdc are shown in Figure 6. Device current as a function of temperature and voltage was similar in all three bias circuits. Maximum rated voltage (15 Vdc) could be maintained across the device at temperatures up to 270°C, and device current was stable at values below 2 milliamps at temperatures up to 270°C. Device current appeared to be somewhat higher with the inputs high, but the difference was not considered important. Consequently, Circuit "C", which has inputs both high and low, was tentatively selected as the accelerated life test circuit. This circuit was selected because it stresses both n and p-channel gate oxides. Circuit "A" only stresses the p-channel oxide, and Circuit "B" only stresses the n-channel oxide.

4.2 Junction Temperature Studies

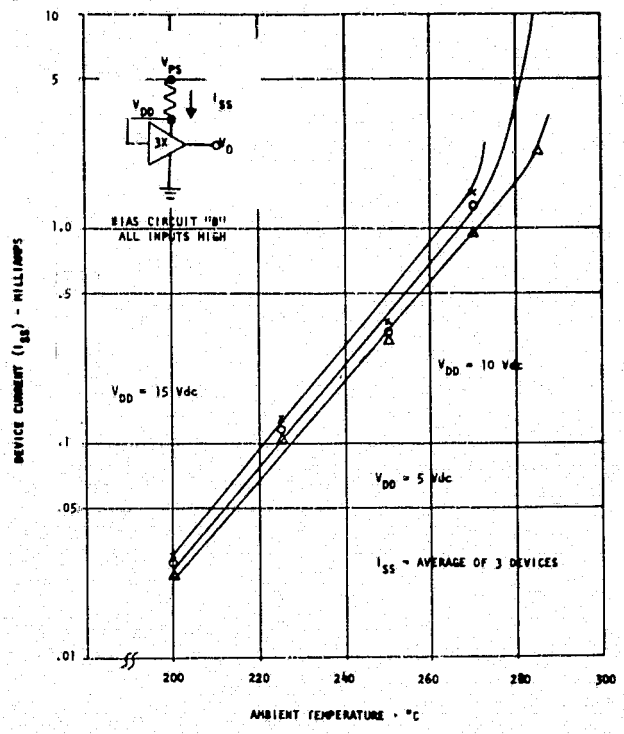
Since microcircuit lifetimes are a function of junction temperature, studies were conducted to determine junction temperatures of devices when operated in the selected bias circuit at ambient temperatures up to 270°C. Both infrared and electrical test techniques were used to study device thermal characteristics.

During the infrared studies, microcircuits were operated in the selected bias circuit at ambient temperatures between 200°C and 270°C using specially constructed micro-ovens. Thermal maps of the chip surface were constructed from radiance data taken with a Barnes RM-50 Infrared Microscanner using a delta radiance procedure. This procedure involved scanning the chip surface in an unpowered condition at a known ambient temperature and recording the detector output. The microcircuit was then powered with 15 Vdc and a second scan obtained. The resultant temperature increase was calculated from the change in detector output between the two scans. Less than 1°C temperature rise over ambient was observed at any point on the chip surface.

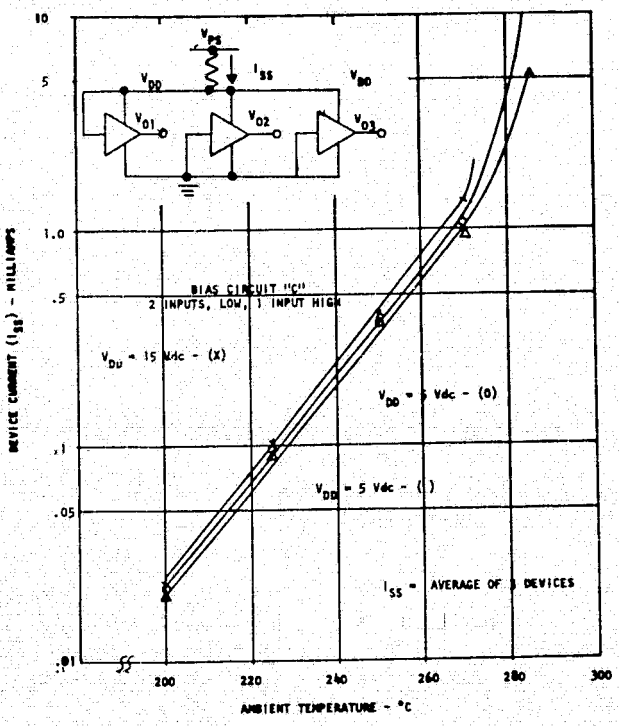
An electrical test technique was also utilized to determine the maximum junction temperature of microcircuits when operated at 15 Vdc in the intended life test fixtures and ovens. Use of the electrical technique minimizes the error in junction temperature determination due to the microcircuit mounting method and air velocity in the life test chamber. The forward voltage of an



BIAS CIRCUIT A



BIAS CIRCUIT B



BIAS CIRCUIT C

FIGURE 6. BIAS CIRCUIT EVALUATION RESULTS

input protective diode was used as a temperature sensitive parameter to determine maximum junction temperatures using a technique similar to MIL-STD-883, Method 1012, Condition C. Measurements of forward voltage were accomplished at ambient temperatures between 200°C and 270°C. Less than 1°C rise over the ambient temperature was calculated for all test conditions.

4.3 Step Stress Tests

Step-stress testing was performed to: (1) validate the nondestructive nature of the selected high temperature bias circuit, and (2) obtain sufficient failure data on a reasonable quantity of microcircuits to make a final determination of the accelerated test conditions. Formal step-stress tests were performed with 20 Lot A microcircuits operated at 15 Vdc at ambient temperatures between 200°C and 270°C. Each step duration was 16 hours with the ambient temperature generally increased in 25°C increments. Insufficient Lot B devices were available to perform a step-stress test.

In addition to the electrical parameter measurements performed at 25°C after cool-down with bias applied at the completion of each step, device currents and output voltages were monitored at each temperature step. Figure 7 shows the results of the formal step-stress tests with Lot A devices in terms of device current, voltage and number of failures experienced at each step. The currents and voltages observed during the step-stress test are similar to those observed during bias circuit evaluations, and represent anticipated device performance during the accelerated life tests. Only four (4) device failures were observed during the step-stress test. These four failures were detected during electrical tests following the 200°C step. All failures were attributed to cation drift in the gate oxide of n-channel transistors.

4.4 Life Test Conditions

Evaluation of the prior circuit evaluations, thermal studies and step-stress tests indicated that the selected bias circuit was suitable for life testing at ambient temperatures up to 270°C. Maximum rated voltage (15 Vdc) is maintained across the device with less than 2 milliamps of device current, and both n and p-channel gate oxides are stressed. Junction temperatures are also within 1°C of ambient.

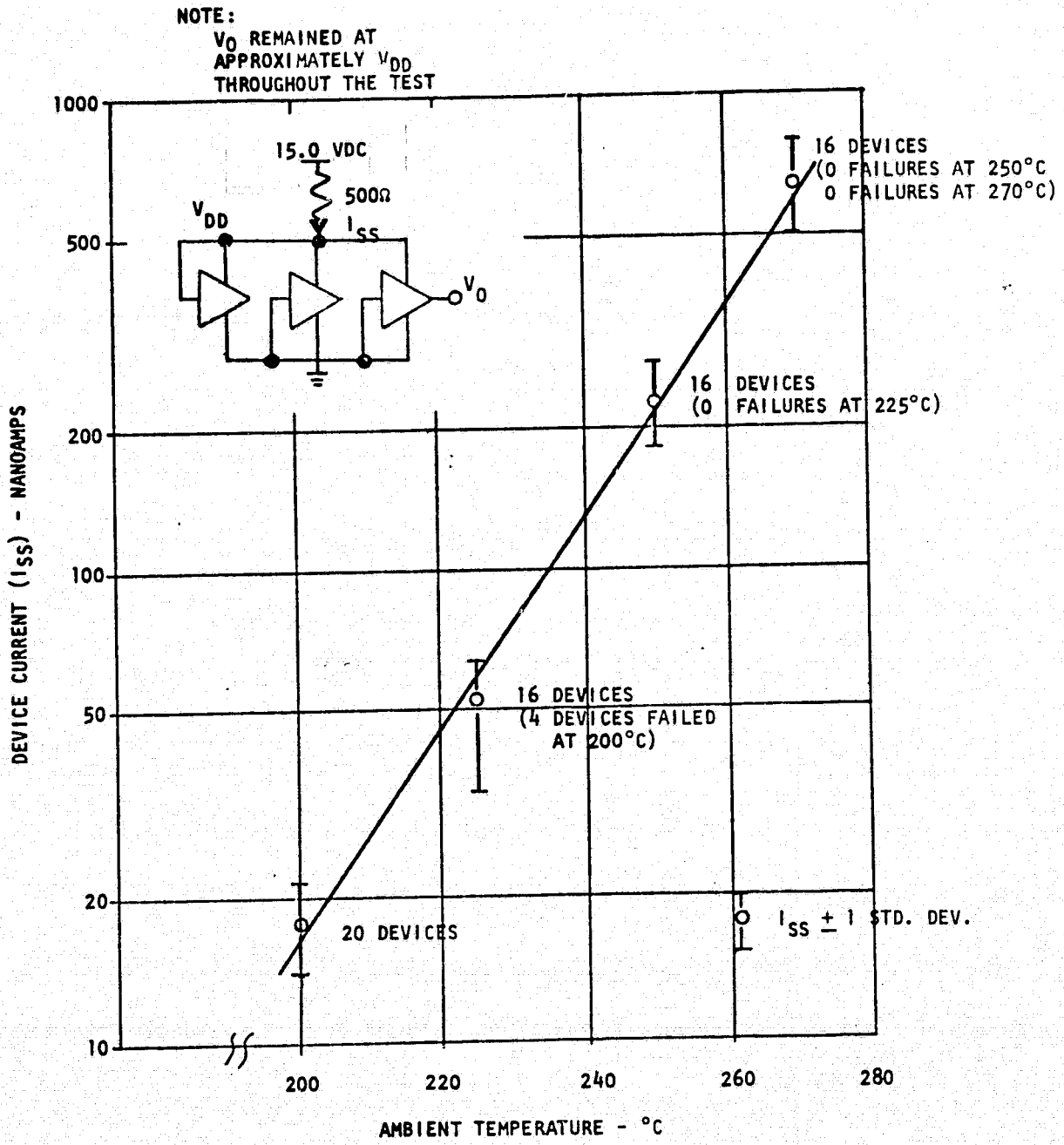
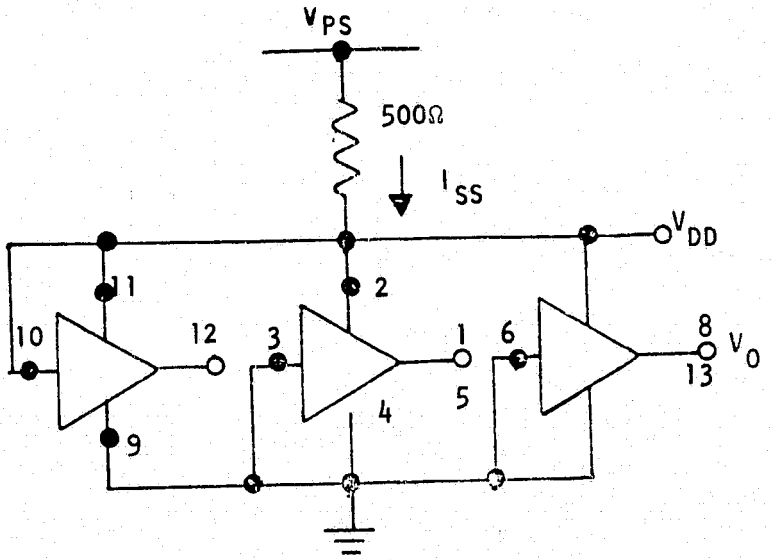


FIGURE 7. STEP-STRESS TEST RESULTS - LOT A

Although no device failures were experienced after the 200°C step of the step-stress tests, it was decided to limit the maximum life test temperature to 250°C to assure oven availability. Thus, with 250°C established as the maximum test temperature, 225°C and 200°C were selected as the mid and low temperature conditions. A minimum of 25°C separation between test temperatures is desirable to minimize errors in subsequent calculations of acceleration factors from the life test data. Bias voltages of 5 Vdc, 10 Vdc, and 15 Vdc were also selected for similar reasons. Figure 8 shows the final bias circuit configuration, and the approximate values of device voltage, current, power dissipation and junction temperature for each life test.



TEST CELL NUMBER	T_A AMBIENT TEMPERATURE (°C)	V_{DD} DEVICE VOLTAGE (VOLTS)	I_{SS} DEVICE CURRENT (MICRO AMPS)	P_d POWER DISSIPATION (MILLI WATTS)	T_J JUNCTION TEMPERATURE (°C)
101	250	15	255	3.8	251.9
201	250	10	215	2.2	250.6
301	250	5	170	0.9	250.2
102	225	15	70	1.0	225.3
202	225	10	55	0.6	225.2
103	200	15	20	0.3	200.1

1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES FOR LOT A AND LOT B DEVICES.
2. JUNCTION TEMPERATURES BASED ON AN ESTIMATED THERMAL RESISTANCE (θ_{JA}) OF 250°C/WATT

FIGURE 8. SUMMARY OF LIFE TEST CONDITIONS

5.0 LIFE TEST RESULTS

The cumulative number of Lot A device failures observed in each test cell and at each electrical measurement point is shown in Table 3. This table also shows the cumulative number of failures due to surface instability problems, internal wire-to-die shorts, and cracked packages. A more detailed summary of failure modes and mechanisms is provided in Table 4, and Appendix C contains a complete description of failure analysis findings. Note the large number of failures due to cracked packages. Sixty-three percent (63%) of the total Lot A device failures (192 total failed devices) were attributed to fractured glass seals which allowed moisture to enter the package. An additional nine percent (9%) of the total failures were due to internal wire-to-die shorts, leaving only twenty-eight percent (28%) of the total failures for an analysis of voltage stress effects. The five to thirteen surface related failures in each test cell were not sufficient for a statistical analysis of voltage stress effects on microcircuit failure rates. Consequently, the life test matrix was repeated with Lot B devices.

The results of the Lot B life tests are summarized in Tables 5 and 6. No package related failures were experienced with Lot B devices. However, approximately the same number of Lot A and Lot B devices failed due to internal wire-to-die shorts. Seventeen (17) Lot A failures and sixteen (16) Lot B failures were due to wire-to-die shorts. There were also a number of Lot B failures due to bulk silicon defects (18 failed devices), and test errors (2 failed devices); leaving a total of fifty-eight (58) failed devices for analysis of voltage stress effects. Again, as with Lot A, the total number of failures due to surface related problems was not sufficient for a meaningful statistical analysis.

Combining the Lot A and Lot B surface related failure data results in a data set that can be used for a limited statistical analysis of voltage stress effects. However, the combined sample size of devices on test must be censored to eliminate all nonsurface related failures, and consideration must be given to the different end-point limits used as failure criteria for Lot A and Lot B devices. The combined data set is shown in Table 7 for the three major surface related failure mechanisms observed during the test program.

TABLE 3. TEST SUMMARY - LOT A

CELL NO	TEMP °C	VOLTS Vdc	NO. ON TEST [1]	FAIL MODE	CUMULATIVE NO. OF FAILURES AT HOURS OF TEST													
					1	2	4	8	16	32	64	128	256	512	1000	2000	3000	4000
101	250	15	40	S.I. [2]	5	6	6	6	6	6	6	7	13	13	13	13	TEST DISCON-TINUED	
				W.S. [3]	0	0	0	0	1	1	2	2	2	2	2	2		
				C.P. [4]	0	0	0	0	0	0	0	0	1	1	15	20		
				TOTAL	5	6	6	6	7	7	8	9	16	16	30	35		
201	250	10	40	S.I.	10	10	10	10	10	10	10	10	10	10	10	10	TEST DISCON-TINUED	
				W.S.	1	1	2	2	3	3	3	4	4	4	4	4		
				C.P.	0	0	0	0	0	0	0	0	1	2	16	23		
				TOTAL	11	11	12	12	13	13	13	14	15	16	30	37		
301	250	5	40	S.I.	9	9	9	9	9	9	9	9	9	9	9	9	9	TEST DISCON-TINUED
				W.S.	0	1	2	2	2	2	2	3	3	3	3	3	3	
				C.P.	0	0	0	0	0	0	0	0	0	0	0	13	9	
				TOTAL	9	10	11	11	11	11	11	12	12	12	12	15	21	
102	225	15	40	S.I.	5	7	7	7	8	8	8	9	9	9	9	9	TEST DISCON-TINUED	
				W.S.	0	1	1	1	1	1	2	3	3	3	3	3		
				C.P.	0	0	0	0	0	0	0	0	1	8	9	23		
				TOTAL	5	8	8	8	9	9	10	12	13	20	21	35		
202	225	10	40	S.I.	4	5	5	5	5	5	5	5	5	5	5	5	5	TEST DISCON-TINUED
				W.S.	2	2	2	2	2	2	2	2	2	2	2	2	2	
				C.P.	0	0	0	0	0	0	0	0	0	0	0	14	23	
				TOTAL	6	7	7	7	7	7	7	7	7	7	7	21	30	
103	200	15	40	S.I.	1	2	5	7	8	8	8	8	8	8	8	8	8	TEST DISCON-TINUED
				W.S.	1	1	1	1	2	2	2	3	3	3	3	3	3	
				C.P.	0	0	0	0	0	0	0	0	0	2	8	17	23	
				TOTAL	2	3	6	8	10	10	10	11	11	13	19	28	34	

[1] ALL DEVICES ARE 4007, CMOS-DUAL COMPLEMENTARY PAIR PLUS INVERTER
[2] S.I. = SURFACE INSTABILITY
[3] W.S. = WIRE-TO-DIE SHORT
[4] C.P. = CRACKED PACKAGE

TABLE 4. FAILURE MODE/MECHANISM SUMMARY - LOT A

	FAILURE CATEGORY NO. ⚠	FAILURE MODE/FAILURE MECHANISM	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL					
			250°C			225°C		200°C
			15V	10V	5V	15V	10V	15V
			101	201	301	102	202	103
MECHANICAL FAILURES	1	WIRE-TO-DIE SHORT/WIRE SAG PLUS Al-Si ALLOYING	1 @ 16 1 @ 64	1 @ 1 1 @ 4 1 @ 16 1 @ 128	1 @ 2 1 @ 4 1 @ 128	1 @ 2 1 @ 64 1 @ 128	2 @ 1	1 @ 1 1 @ 16 1 @ 128
	2	PIN-PIN LEAKAGES, OPEN WIRE BONDS, AND/OR V_{TH} DECREASES/FRACTURED GLASS SEAL DUE TO THERMAL EXPANSIONS WHICH ALLOWED MOISTURE TO ENTER THE PACKAGE.	1 @ 256 14 @ 1000 5 @ 2000	1 @ 256 1 @ 512 14 @ 1000 7 @ 2000	3 @ 2000 6 @ 3000	1 @ 256 7 @ 512 1 @ 1000 14 @ 2000	14 @ 2000 9 @ 3000	2 @ 512 6 @ 1000 9 @ 2000 6 @ 3000
SURFACE INSTABILITY FAILURES	5	LOW V_{TH} AND HIGH I_{DSS}, Q4-Q5-Q6/CATION DRIFT I	5 @ 1 1 @ 2	10 @ 1	9 @ 1	5 @ 1 2 @ 2 1 @ 16	4 @ 1 1 @ 2	1 @ 1 1 @ 2 3 @ 4 2 @ 8 1 @ 16
	7	HIGH V_{TH}, Q1-Q2/SLOW TRAPPING	1 @ 128 6 @ 256			1 @ 128		
		TOTAL NUMBER OF FAILED PARTS	35	37	21	35	30	34

⚠ REFERS TO TABLE C1 OF APPENDIX C WHICH GIVES DETAILED RESULTS OF FAILURE ANALYSIS.

TABLE 5. TEST SUMMARY - LOT B

CELL NO	TEMP °C	VOLTS Vdc	NO. ON TEST[1]	FAIL MODE	CUMULATIVE NO. OF FAILURES AT HOURS OF TEST													
					1	2	4	8	16	32	64	128[4]	256	512	1000	2000	3000	4000
101	250	15	35	S.I.[2]	4	5	6	6	7	7	7	8	8	8	8	8	8	10
				OTHER[3]	1	2	2	2	2	4	4	5	6	6	6	7	7	7
				TOTAL	5	7	8	8	9	11	11	13	14	14	14	15	15	17
201	250	10	35	S.I.	1	1	1	1	2	3	4	7	7	8	9	12	12	13
				OTHER	0	0	0	2	2	2	3	3	3	3	4	5	6	6
				TOTAL	1	1	1	3	4	5	7	10	10	11	13	17	18	19
301	250	5	35	S.I.	1	1	1	1	1	2	3	4	4	4	7	7	7	7
				OTHER	0	0	0	0	1	1	1	2	2	2	3	3	3	4
				TOTAL	1	1	1	1	2	3	4	6	6	6	10	10	10	11
102	225	15	35	S.I.	3	3	3	3	3	3	4	5	7	8	10	11	11	12
				OTHER	1	1	1	1	1	2	3	4	4	4	4	4	4	4
				TOTAL	4	4	4	4	4	5	7	9	11	12	14	15	15	16
202	225	10	35	S.I.	1	1	1	1	1	1	2	2	2	2	2	3	3	3
				OTHER	2	4	5	6	7	7	7	10	11	11	11	11	11	11
				TOTAL	3	5	6	7	8	8	9	12	13	13	13	14	14	14
103	200	15	35	S.I.	6	7	7	7	7	7	7	7	7	9	9	11	11	13
				OTHER	0	1	1	1	1	2	2	3	3	4	4	4	4	4
				TOTAL	6	8	8	8	8	9	9	10	10	13	13	15	15	17

[1] ALL DEVICES ARE 4007, CMOS-DUAL COMPLEMENTARY PAIR PLUS INVERTER
[2] S.I. - SURFACE INSTABILITY
[3] INCLUDES ALL NON-SURFACE RELATED FAILURES.
[4] TEST TIME FOR CELLS 100, 201 & 301 IS 200 HOURS.

TABLE 6. FAILURE MODE/MECHANISM SUMMARY - LOT B

	FAILURE CATEGORY NO. ⚠	FAILURE MODE/FAILURE MECHANISM	QUANTITY OF FAILURES AND TIME OF FAILURES (HOURS) BY TEST CELL					
			250°C			225°C		200°C
			15V	10V	5V	15V	10V	15V
			101	201	301	102	202	103
BULK AND MECHANICAL FAILURES	1	WIRE-TO-DIE SHORT/WIRE SAG PLUS Al-Si ALLOYING	1 @ 1 1 @ 2 1 @ 32 1 @ 128	1 @ 8 1 @ 3000	1 @ 16 1 @ 1000	1 @ 1	1 @ 1 1 @ 2 1 @ 4 1 @ 8 1 @ 16	1 @ 2 1 @ 32
	3	HIGH $V_{DS(ON)}$, Q4 (N-CHAN) AND/OR Q1 (P-CHAN)/INCREASE IN THE SOURCE OHMIC CONTACT RESISTANCE	1 @ 32 1 @ 256	1 @ 8 1 @ 64	1 @ 128 1 @ 4000	1 @ 32 1 @ 64 1 @ 128	1 @ 1 3 @ 128 1 @ 256	1 @ 128 1 @ 512
	4	OPEN PIN/LIFTED BOND DUE TO KIRKENDALL VOIDING IN $AuAl_2$		1 @ 1000 1 @ 2000				
SURFACE INSTABILITY FAILURES	5	LOW V_{TH} AND HIGH I_{DSS}, Q4-Q6/ CATION DRIFT I	2 @ 1	1 @ 1 1 @ 128	1 @ 1	2 @ 1	1 @ 1	6 @ 1
	6	HIGH I_{DSS}, Q4-Q6/CATION DRIFT II	1 @ 1 1 @ 2 1 @ 4 1 @ 16 1 @ 128	1 @ 16 1 @ 32 1 @ 64	1 @ 32 1 @ 64 1 @ 128 1 @ 1000	1 @ 1 1 @ 64	1 @ 64 1 @ 2000	1 @ 2 2 @ 512
	9	DEGRADED P-WELL JUNCTION AND CR7-8/ R3/ION MIGRATION		1 @ 2000				
	8	DRAIN-SOURCE PUNCH-THROUGH, Q1-Q2 OR DEGRADED Q3 DRAIN JUNCTION/ION MIGRATION	1 @ 1	2 @ 2000	1 @ 1000	1 @ 128 1 @ 256		
	7	HIGH $V_{DS(ON)}$, Q1-Q2/V_{TH} INCREASE DUE TO SLOW TRAPPING (ALSO DUE IN PART TO CATEGORY 3 MECHANISM)	2 @ 4000	2 @ 128 1 @ 512 1 @ 1000 1 @ 4000	1 @ 1000	1 @ 256 1 @ 512 2 @ 1000 1 @ 2000 1 @ 4000		2 @ 2000 2 @ 4000
TEST ERROR	10	OPEN PIN/ACCIDENTAL LEAD DAMAGE					1 @ 2	
	11	OPEN PINS/ALUMINUM ELECTROMIGRATION	1 @ 2000					
		TOTAL NUMBER OF FAILED PARTS	17	19	11	16	14	17

⚠ REFERS TO TABLE C1 OF APPENDIX C WHICH GIVES DETAILED RESULTS OF FAILURE ANALYSIS.

TABLE 7. SURFACE RELATED FAILURES - LOT A & B

CELL NO	TEMP °C	VOLTS Vdc	NO. ON TEST [1]	FAIL MECH	CUMULATIVE NO. OF FAILURES AT HOURS OF TEST													
					1	2	4	8	16	32	64	128	256	512	1000	2000	3000	4000
101	250	15	46	ION DRIFT [2]	8	10	11	11	12	12	12	13	13	13	13	13	13	13
				MIGRATION [3]	1	1	1	1	1	1	1	1	1	1	1	1	1	1
				SLOW HOLE [4]	0	0	0	0	0	0	0	1	7	7	7	7	7	9
				TOTAL	9	11	12	12	13	13	13	15	21	21	21	21	21	23
201	250	10	42	ION DRIFT	11	11	11	11	12	13	14	15	15	15	15	15	15	15
				MIGRATION	0	0	0	0	0	0	0	0	0	0	0	3	3	3
				SLOW HOLE	0	0	0	0	0	0	0	2	2	3	4	4	4	5
				TOTAL	11	11	11	11	12	13	14	17	17	18	19	22	22	23
301	250	5	59	ION DRIFT	10	10	10	10	10	11	12	13	13	13	14	14	14	14
				MIGRATION	0	0	0	0	0	0	0	0	0	0	1	1	1	1
				SLOW HOLE	0	0	0	0	0	0	0	0	0	0	1	1	1	1
				TOTAL	10	10	10	10	10	11	12	13	13	13	16	16	16	16
102	225	15	45	ION DRIFT	8	10	10	10	11	11	12	12	12	12	12	12	12	12
				MIGRATION	0	0	0	0	0	0	0	1	2	2	2	2	2	2
				SLOW HOLE	0	0	0	0	0	0	0	1	2	3	5	6	6	7
				TOTAL	8	10	10	10	11	11	12	14	16	17	19	20	20	21
202	225	10	39	ION DRIFT	5	6	6	6	6	6	7	7	7	7	7	8	8	8
				MIGRATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				SLOW HOLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				TOTAL	5	6	6	6	6	6	7	7	7	7	7	8	8	8
103	200	15	45	ION DRIFT	7	9	12	14	15	15	15	15	15	17	17	17	17	17
				MIGRATION	0	0	0	0	0	0	0	0	0	0	0	0	0	0
				SLOW HOLE	0	0	0	0	0	0	0	0	0	0	0	2	2	4
				TOTAL	7	9	12	14	15	15	15	15	15	17	17	19	19	21

[1] NO. ON TEST IS TOTAL DEVICES PLACED ON TEST MINUS ALL NON-SURFACE RELATED FAILURES.
[2] ION DRIFT = CATION DRIFT I & II (FAILURE CATEGORIES 5 & 6)
[3] MIGRATION = ION MIGRATION (FAILURE CATEGORIES 8 & 9)
[4] SLOW HOLE = SLOW HOLE TRAPPING (FAILURE CATEGORY 7)

A combined summary of all failure modes/mechanisms observed during the program is shown in Table 8. Except for the Lot A cracked packages, the failure modes/mechanisms in Lot A and Lot B were similar. There were approximately the same number of wire-to-die shorts, and surface related defects in Lot A and Lot B. Examination of the number of failures in subcategories of surface related mechanisms indicates cation drift in SiO_2, and slow hole trapping at Si/SiO_2 interfaces were observed in both Lot A and Lot B devices. However, surface ion migration and bulk silicon defects were only observed in Lot B devices. The occurrence of package cracks may have masked the ion migration and bulk silicon problems in Lot A devices. Examination of the data in Table 7 also shows that most of the cation drift failures occurred early in the test, while the ion migration and slow hole trapping type failures did not occur until later in the test, suggesting the possibility of two distinct failure distributions.

TABLE 8. COMBINED FAILURE MODE/MECHANISM SUMMARY

FAILURE MODE/MECHANISM	NO. OF FAILURES			
			TOTAL	
	LOT A	LOT B	NO.	%
SURFACE EFFECTS	54	58	112	39.2
o CATION DRIFT	46	33	79	27.6
o ION MIGRATION	0	7	7	2.5
o SLOW HOLE TRAPPING	8	18	26	9.1
CRACKED PACKAGES	121	0	121	42.3
WIRE-TO-DIE SHORTS	17	16	33	11.5
BULK SILICON & OTHER DEFECTS	0	20	20	7.0
TOTAL	192	94	286	100.0%

6.0 ANALYSIS OF LIFE TEST DATA

In-depth statistical analyses of the failure data derived from the Lot A and Lot B accelerated life tests were performed to describe the 4007 life characteristics as a function of both temperature and voltage. The basic failure data was previously presented in Table 7, and is limited to only surface related failures. Failures due to package cracks, wire-to-die shorts, bulk silicon defects and test errors are not voltage dependent, and were excluded from an analysis of voltage stress effects. Analysis of the surface related failure data included a determination of: a) the distribution of failure times at each temperature/voltage condition, b) Arrhenius reaction rate model parameters for device aging characteristics as a function of temperature, but at a fixed voltage, c) Eyring reaction rate model parameters for device aging characteristics as a function of temperature and voltage, and d) device failure rates at 125°C and 50°C as a function of voltage, both with and without burn-in.

6.1 Failure Distributions

Analysis of the cumulative percentage failures observed at each test interval, using the techniques previously developed by the Bell Telephone Laboratories [2, 5], resulted in insufficient failure time resolution to accurately determine the distribution of failure times. Consequently, a failed parameter interpolation technique was used to estimate an exact failure time for each failed device. This technique is illustrated in Figure 9, and consists of fitting an equation to values of the failed parameter at test intervals prior to and including the test interval that the failed value was observed. The resulting equation is then used to calculate an operating time at which the failed parameter was equal to the specified end-point limit. Failed parameters, specification limits, and the end-point limits used to interpolate failure times are shown in Table 9. In order to combine Lot A and Lot B data in a consistent fashion, it was necessary to use the same end-point limits for each failed parameter that was observed in both Lot A and Lot B. Devices that exhibited out-of-tolerance device current (I_{SS}) presented no problem, since the parameter limits and measurement conditions were identical for Lot A and Lot B. However, the Lot A "V_{O3}" output voltage and Lot B "V_{DD} - V_{OH3}" output voltage have different end-point limits although they are equivalent parameters, and are

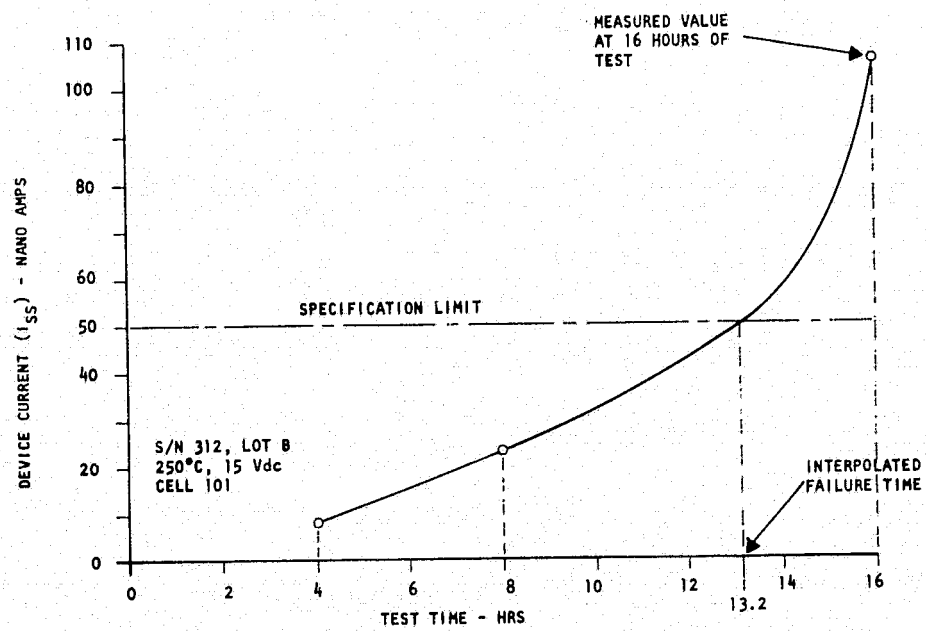


FIGURE 9. EXAMPLE OF FAILURE TIME INTERPOLATION

TABLE 9. FAILURE CRITERIA FOR PARAMETER INTERPOLATION

LOT NO.	PARAMETER	SPECIFICATION LIMIT	ANALYSIS LIMIT
A & B	I_{SS}	50 nA max	50 nA max
A	V_{O3}	10 mV max	10 mV max
B	$V_{DD} - V_{OH3}$	50 mV max	10 mV max
A	V_{OH1}	3.6 Vdc min	$\Delta V_{TH} \geq 0.36$ Vdc
B	V_{OH2}	4.0 Vdc min	4.0 Vdc min

measured in an identical fashion. Consequently, the Lot B "V_{DD} - V_{OH3}" parameter limit was changed from 50 mV maximum to the Lot A "V_{O3}" parameter limit of 10 mV maximum to permit consistent interpolation of failure times for both Lot A and Lot B devices. The Lot A "V_{OH1}" and Lot B "V_{OH2}" are also comparable parameters, but were measured under different test conditions, and had different end-point limits. Since both Lot A "V_{OH1}" and Lot B "V_{OH2}" failures were due to threshold voltage shifts (ΔV_{TH}), a ΔV_{TH} limit was established for the Lot A "V_{OH1}" failures. The established limit of 0.36 Vdc is equal to the average ΔV_{TH} observed in Lot B "V_{OH2}" failures.

Once exact failure times were interpolated for each failed device, the nature of the failure distribution at each temperature/voltage condition was examined. Plots of cumulative percentage failures on a normal probability scale versus log failure time resulted in "S" shaped curves, indicating bimodal failure distributions. Evaluation of these distributions indicated that the bimodal cumulative distribution function (Cdf {life}) could be represented by two log-normal distributions, a "freak" and a "main", as follows:

$$\text{Cdf }\{\text{life}\}_{\text{Total}} = [\text{Cdf }\{\text{life}\}_{\text{freak}}]\,[\%_F] + [\text{Cdf }\{\text{life}\}_{\text{main}}]\,[\%_M] \qquad (1)$$

where:

$\%_F$ = the percentage of the total population that is described by the "freak" distribution

$\%_M$ = the percentage of the total population that is described by the "main" distribution

$$\text{Cdf }\{\text{life}\} = \frac{1}{\sigma\sqrt{2\pi}} \int_0^t \frac{1}{t'} \exp\left[- \frac{\left(\log_e (t') - \mu\right)^2}{2\sigma^2} \right] dt' \qquad (2)$$

where:

μ = $\log_e$ (median life)

σ = standard deviation of $\log_e$ (life)

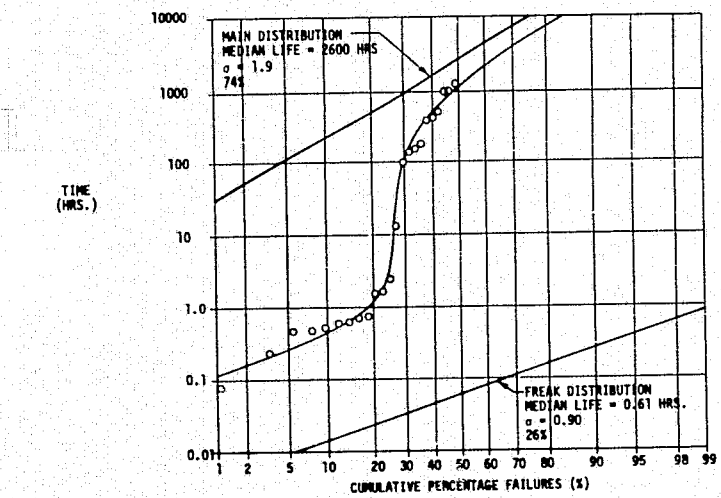
t = use time

A first order approximation of numerical values for "freak" and "main" percentages, median lifetimes and standard deviations was obtained using the graphical technique described by Peck [5]. Using the parameter values obtained from the graphical solution as a starting point, a computer aided technique was used to iterate the unknowns in equations (1) and (2) until the calculated probability at each test time closely compared to the observed cumulative percentage failure. The iteration process was considered complete when both the sum of the differences between the calculated and observed probability, and the maximum difference between the calculated and observed probability at any time was minimized.

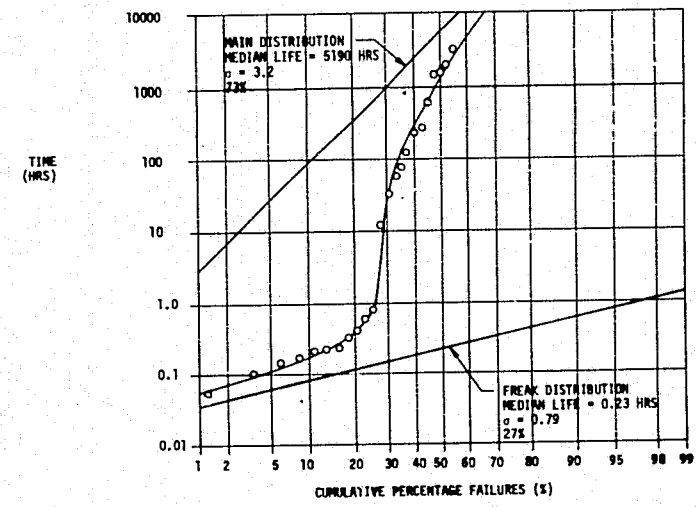
The results of these analyses are shown in Figures 10 and 11. The plotted data points represent the interpolated failure time for each failed device. The solid "S" shaped curves represent solutions to equation (1) using the median life times, standard deviations and percentages for the "freak" and "main" lognormal distributions represented by the straight line plots. As can be seen from the plots for each combination of temperature and voltage, the calculated "S" shaped curves representing the Cdf {life} for the combined "freak" and "main" lognormal distributions provide a reasonable representation of the interpolated failure data. Also, by combining Lot A and Lot B failure data, and interpolating failure times, "freak" and "main" distribution parameters could be determined for all but one of the test conditions. Insufficient data was available to determine a median life and standard deviation for the "main" distribution at the 225°C, 10 Vdc condition.

A summary of the calculated failure distribution parameters is shown in Table 10. Statistical tests of significance [6] using these parameters indicated the following:

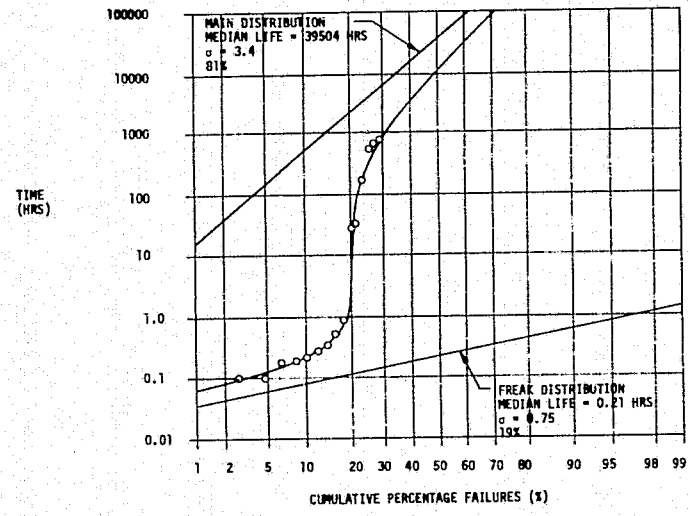
- o median lifetimes of the "freak" and "main" distributions are related to temperature, but the standard deviations are independent of temperature
- o median lifetimes and standard deviations of the "main" distribution are related to voltage
- o median lifetimes and standard deviations of the "freak" distribution are not dependent upon voltage (this unexpected result is discussed in the following text)



250°C, 15 VOLT - CELL 101

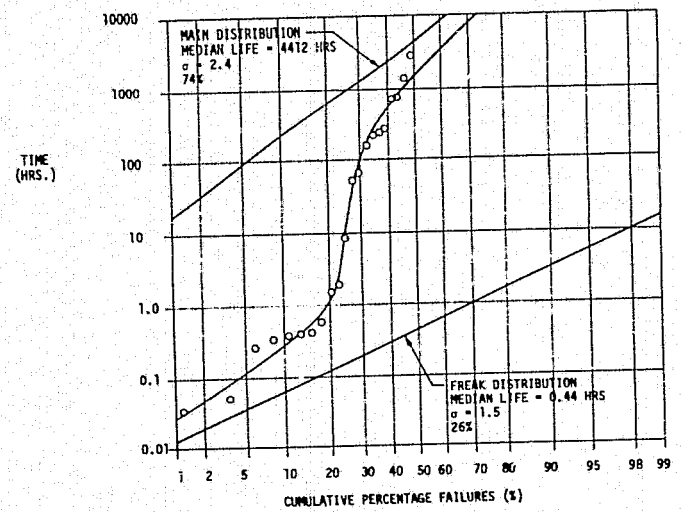


250°C, 10 VOLT - CELL 201

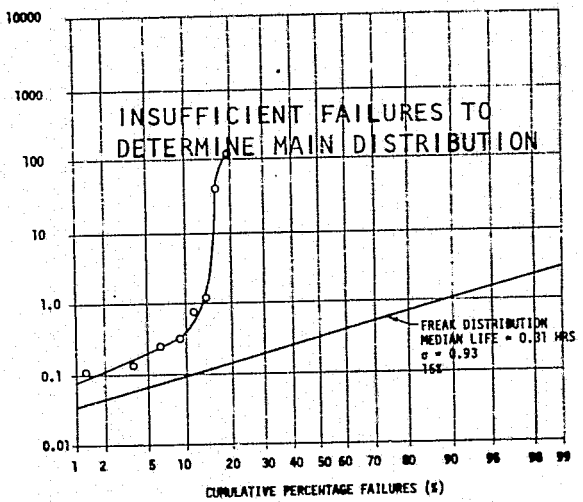


250°C, 5 VOLTS - CELL 301

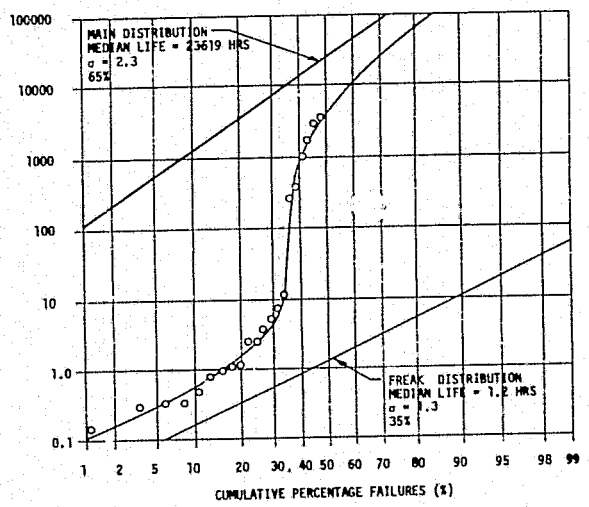
FIGURE 10. FAILURE DISTRIBUTIONS AT 250°C



225°C, 15 VOLT - CELL 102



225°C, 10 VOLT - CELL 202



200°C, 15 VOLT - CELL 103

FIGURE 11. FAILURE DISTRIBUTIONS AT 225°C & 200°C

TABLE 10. SUMMARY OF FAILURE DISTRIBUTION PARAMETERS

CELL NO.	TEMP. °C	VOLTS Vdc	PERCENT FREAK %	MEDIAN LIFE - HRS		STANDARD DEVIATION	
				FREAK	MAIN	FREAK	MAIN
101	250	15	26	0.61	2,600	0.90	1.9
201	250	10	27	0.23	5,190	0.79	3.2
301	250	5	19	0.21	39,504	0.75	3.4
102	225	15	26	0.44	4,412	1.50	2.4
202	225	10	15	0.93	-	0.93	-
103	200	15	35	1.20	23,619	1.30	2.3

- the range of percentage "freaks" observed in each life test is due to sampling variations

Based on the preceeding observations, the following parameters were calculated for use in subsequent analyses:

- average percent of "freak" devices in the overall test population = 24.6%
- pooled standard deviations (σ_p) [7] of:
  - σ_p for "freak" distributions = 1.50
  - σ_p for "main" 15 volt distributions = 2.16
  - σ_p for "main" 10 volt distributions = 3.15
  - σ_p for "main" 5 volt distributions = 3.41

The use of an average value of percentage "freaks" in the test population and constant standard deviation as a function of temperature is in agreement with prior test observations and assumptions [1, 2]. The generally increasing standard deviation of the "main" distribution with decreasing voltage has been observed in other accelerated test evaluations (RADC Contract F30602-73-C-0140), but the physical basis for this effect is not well understood. The lack of a "freak" median lifetime voltage dependence is also not well understood, and was unexpected since almost all of the "freak" population failures were due to cation drift through gate oxides. Applied voltage is required to drift the contaminate ions through the oxide to the SiO_2/Si interface, and the time required for this process to result in device failure is expected to be dependent upon the magnitude of the applied voltage [7]. An explanation for the apparent lack of voltage dependence may be that the interpolated failure times between zero and one hour were not accurate estimates of the actual failure times. Almost all of the "freak" failures were observed at the one (1) hour measurement point, providing little information about the shape of the failed parameter versus time curve. Thus, the calculated failure times were based on a linear interpolation between zero and one hour. However, there is no guarantee that a linear curve shape accurately represents the behavior of the failed devices. Life tests at test temperatures below 200°C may provide better resolution of device failure times, and greater visibility of voltage effects that may exist.

An examination of the types of failures that comprise the "freak" and "main" distributions indicates that the "freak" distributions are almost exclusively due to Type I cation drift failures as described in Appendix C for failure category 5. The "main" distributions result from a combination of primarily slow hole trapping failures (Appendix C, failure category 7) and Cation Drift II type failures (Appendix C, failure category 6). The total number of each type failure mechanism observed in the "freak" and "main" distributions is shown in Table 11.

6.2 Microcircuit Aging Characteristics

Using the median life data derived for the "freak" and "main" failure distributions at each test condition, the applicability of the Arrhenius and Eyring reaction rate models [4] for describing device aging characteristics was examined.

6.2.1 Arrhenius Model - The Arrhenius model describes device lifetime as a function of temperature at a fixed voltage, and may be expressed as follows:

$$t_{50\%} = A \exp\left[\frac{E_A}{k\ Temp}\right] \qquad (3)$$

where:

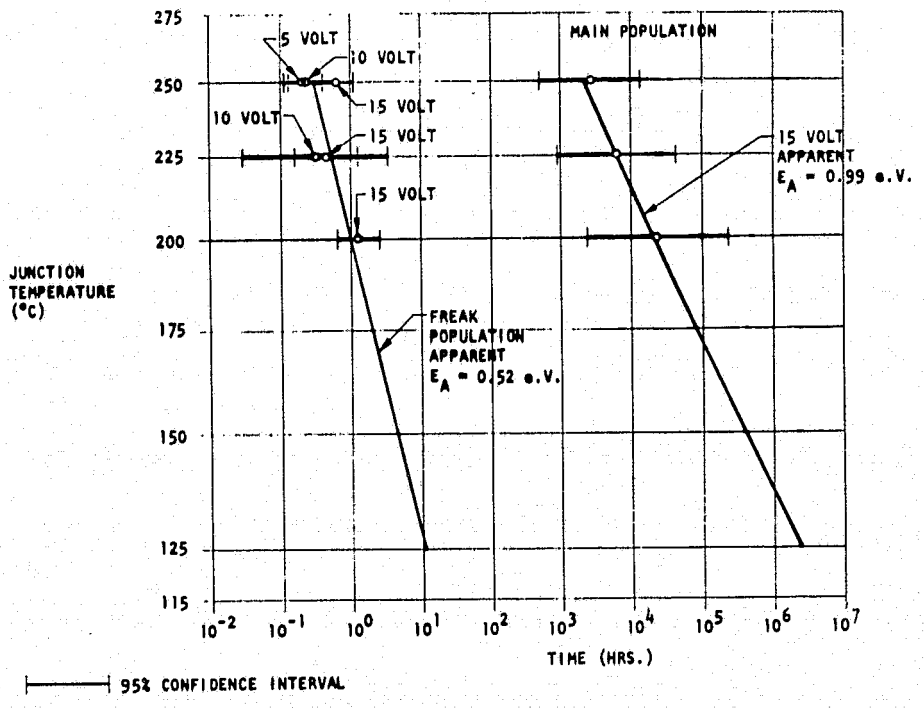
$t_{50\%}$ ≡ device median life at temperature
A ≡ a constant
E_A ≡ apparent activation energy in electron volts
k ≡ Boltzmann's constant = 8.617×10^{-5} eV/K
Temp ≡ absolute junction temperature

Evaluation of the Arrhenius model using the median life data derived from the matrix of accelerated life tests results in the Arrhenius plots shown in Figure 12. The temperature scale for the plots is a linear function of 1/K Temp and the time scale is log (time). Thus, a plot of the Arrhenius equation will appear as a straight line, since

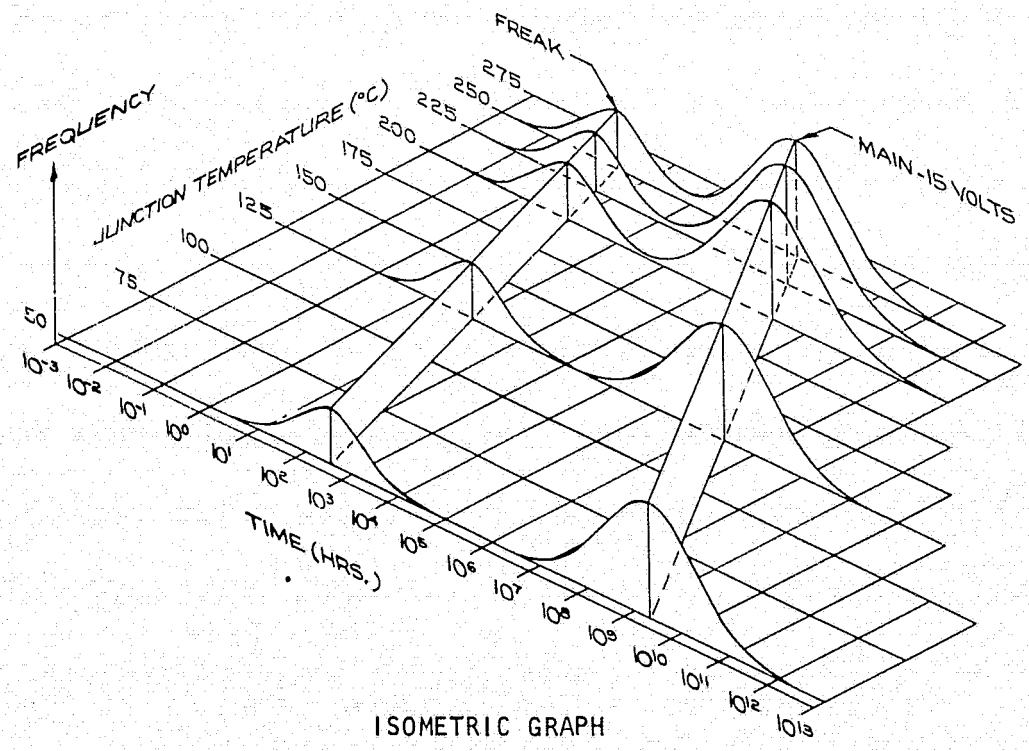
$$\log_e (t_{50\%}) = \log_e (A) + E_A \left(\frac{1}{k\ Temp}\right) \qquad (4)$$

TABLE 11. RELATIONSHIP OF FAILURE MECHANISM TO FAILURE DISTRIBUTIONS

FAILURE MECHANISM	NO. OF FAILED DEVICES		
	FREAK DISTRIBUTION	MAIN DISTRIBUTION	TOTAL
CATION DRIFT I	59	1	60
CATION DRIFT II	6	13	19
SURFACE ION MIGRATION	1	6	7
SLOW HOLE TRAPPING	0	26	26
TOTAL	66	46	112



ARRHENIUS PLOT



ISOMETRIC GRAPH

FIGURE 12. ARRHENIUS PLOT & ISOMETRIC GRAPH

Also shown in Figure 12 is an isometric graph constructed by superimposing the derived probability density functions over the Arrhenius plots. The density functions are based on the average percentages and pooled standard deviations for the "freak" and "main" distributions shown earlier in paragraph 6.1. Examination of the Arrhenius plot in Figure 12 indicates that the Arrhenius model provides a reasonable description of the "freak" distribution median life and the 15 volt "main" distribution median life as a function of temperature. However, there is no significant difference in the observed "freak" median lifetimes for the different voltage conditions. Consequently, the Arrhenius line shown for the "freak" distribution represent the result of a regression analysis using all of the "freak" median lifetimes. The regression analysis yielded the following values for the unknowns A and E_A in the Arrhenius model:

FREAK DISTRIBUTION	MAIN DISTRIBUTION
$A = 2.66 \times 10^{-6}$	$A = 1.57 \times 10^{-6}$
$E_A = 0.52$ eV	$E_A = 0.99$ eV

6.2.2 Eyring Model - The Eyring reaction rate model describes device lifetimes as a function of both temperature and voltage, and may be expressed as [4]:

$$t_{50\%} = \frac{Gh}{Temp} \exp\left\{\frac{E_{TA}}{k\ Temp} - f(V)\left[C + k\ \frac{D}{Temp}\right]\right\} \qquad (5)$$

where:

$t_{50\%}$ ≡ device median life at temperature
G, C, and D are positive constants
E_{TA} ≡ activation energy in electron volts
f(V) ≡ some function of bias voltage
k ≡ Boltzmann's constant = 8.617×10^{-5} eV/K
h ≡ Planck's constant = 1.149×10^{-18} eV hr
Temp ≡ absolute junction temperature

The first step in evaluating the unknowns in equation (5) is to determine the form of the f(V) function. A plot of $\log_e (t_{50\%})$ as a function of voltage, but at a fixed temperature, provides a means for examining the shape of f(V) since,

$$\log_e (t_{50\%}) = \log_e \left[\frac{Gh}{Temp}\right] + \frac{E_{TA}}{Temp} - f(V)\left[C + \frac{D}{k\ Temp}\right] \qquad (6)$$

and at fixed temperature,

$$\log_e (t_{50\%}) = a - b\, f(V) \qquad (7)$$

where:

a and b are constants

Thus, an f(V) function equal to V will appear as a straight line, and other functions can be evaluated using curve fitting techniques. A plot of the 250°C median life data as a function of voltage is shown in Figure 13, and a straight line is a reasonable fit to the observed data. Other forms of f(V) could also be used to represent the data. For example, $f(V) = \frac{1}{V}$, and $f(V) = \log_e (V)$ are both good representations of the observed 250°C data. However, the small number of device failures observed in the "main" distribution results in a large uncertainty about the values of calculated median lifetimes, and selection of one function over the other becomes a matter of engineering judgement at this point in the analysis. The f(V) = V function was selected after the following examination of the Eyring model behavior with these functions:

- o At a small value of voltage, the 1/V function results in a large negative term in the exponent of equation (5), or the equivalent of a negative activation energy. Thus, the 1/V function was rejected on the basis that a negative activation energy can not physically exist.
- o The $f(V) = \log_e (V)$ function has no effect on the apparent activation energy, since a "$\log_e$" term in the exponent of equation (5) becomes a pre-exponential term (i.e., $\exp [\log_e(x)] = X$). Prior studies at McDonnell Douglas (RADC Contract F30602-73-C-0140) had suggested an increase in apparent activation energy with decreasing voltage. Also, as discussed later, the correct form of the Eyring model was not obtained from a multiple linear regression analysis of (6) with $f(V) = \log_e(V)$. Consequently, the $\log_e(V)$ function was rejected.
- o The f(V) = V function results in an increased apparent activation energy with decreasing voltage, and at zero volts the median life is a result of only nonvoltage dependent failure mechanisms. Since all of the failure mechanisms used to determine the "main" distribution median lifetimes were attributed to voltage dependent mechanisms, it would be expected that the the median lifetimes calculated from equation (5) would approach infinity as V approaches zero. Examination of the

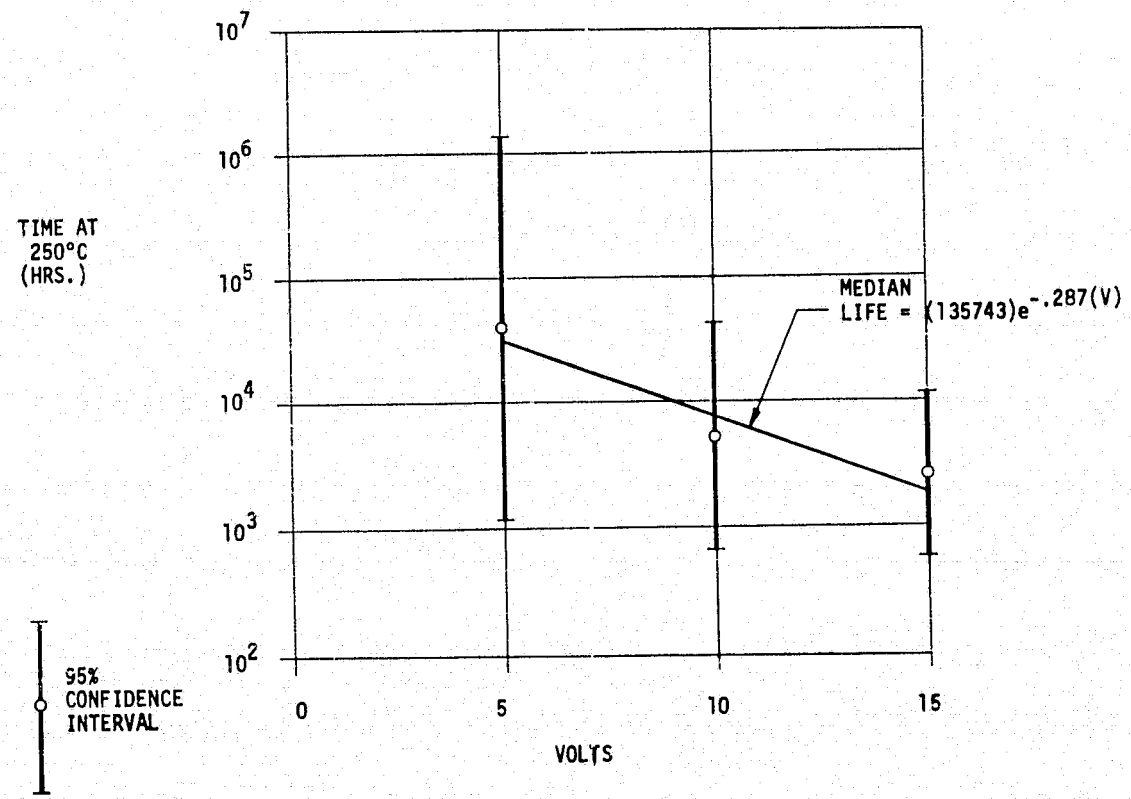


FIGURE 13. VOLTAGE EFFECT AT 250°C

previous plot of $\log_e (t_{50\%})$ versus V in Figure 13 indicates a median life of approximately 10^5 hours at the 250°C, zero volt condition. Insufficient data exists to support or refute a 250°C storage life of this magnitude, but on the basis of the observed failure mechanisms, 10^5 hours is felt to be a conservative estimate of the median life at zero volts. Nevertheless, the f(V) = V function appears reasonable in the normal operating range of 5 to 15 volts, and was used in subsequent evaluations of the Eyring model parameters.

Having selected the form of the f(V) function, the next step in the evaluation would be a determination of the constants C and D in equation (5). These constants could be determined directly from derivatives of (6) with respect to voltage, at two temperatures.

$$\left.\frac{d\,[\log_e (t_{50\%})]}{dV}\right|_{\text{Temp = const.}} = -V\left[C + \frac{D}{k\ \text{Temp}}\right] \qquad (8)$$

Simultaneous solutions of (8) at 250°C and 225°C will yield values for C and D. Although the slope of the $\log_e (t_{50\%})$ versus V function $\left(\frac{d\,[\log_e (t_{50\%})]}{dV}\right)$ is known at 250°C, the lack of a 225°C, 10 volt median life precludes estimating a slope value at 225°C. A multiple linear regression analysis solution of (6) was also not obtainable without an estimate of the 225°C, 10 volt median life. However, a correct form of the Eyring model was obtained from a multiple linear regression analysis of (6) with values of 225°C, 10 volt median lifetimes between 24,000 and 27,000 hours. For these values of median lifetimes, all of the unknowns are positive numbers as required. The value for the constant D is also greater than C which satisfies the condition that the activation energy be greater than the entropy associated with the process [8]. An iterative technique was then used to determine a value for the missing 225°C, 10 volt median life data point that minimized the difference between the calculated median life and the assumed median life at the 225°C, 10 volt condition. In this manner a 26,100 hour estimate of the median life at 225°C and 10 volts was established. The corresponding estimates of the Eyring model unknowns were determined from a regression analysis solution of (6) to be:

E_{TA} = 1.18 eV
G = 2.26 X 10^{10}
C = 3.91 X 10^{-3}
D = 0.1275

Plots of the Eyring equation evaluated at 15, 10 and 5 volts are shown in Figure 14. These plots indicate that the derived Eyring model provides a reasonable representation of the aging characteristics observed for the "main" device population. An isometric graph of the Eyring function and the failure density functions is also shown in Figure 14, and illustrates the change in standard deviation of the failure distributions with applied voltage.

6.3 Failure Rates

As a final step in the analysis of the life test data, device failure rates were calculated at junction temperatures of 125°C and 50°C based on the failure distribution parameters and acceleration factors previously derived. At a given temperature the instantaneous failure rate ($\lambda(t)$) for devices whose lifetimes are lognormally distributed is defined as [9]:

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\sqrt{2\pi}} \exp - \frac{(\log_e (t) - \mu)^2}{2\sigma^2}}{\frac{1}{\sigma\sqrt{2\pi}} \int_t^{\infty} \frac{1}{t'} \left\{ \exp - \frac{\log_e (t') - \mu)^2}{2\sigma^2} \right\} dt'} \qquad (9)$$

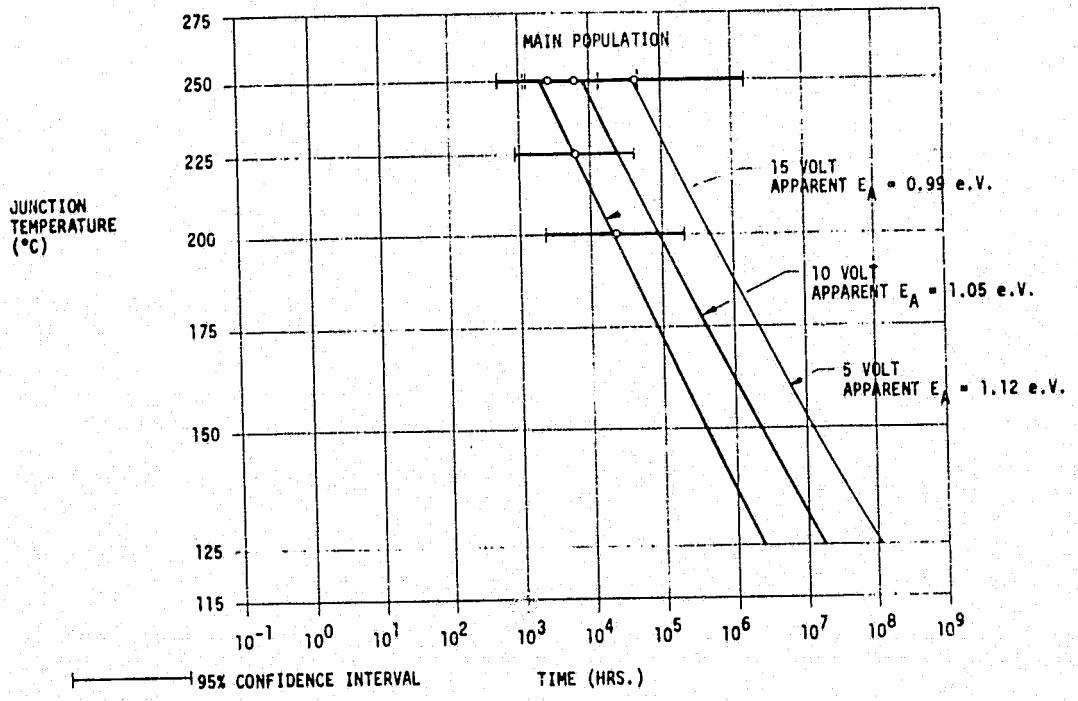
where:

μ = $\log_e$ (median life)
σ = the standard deviation

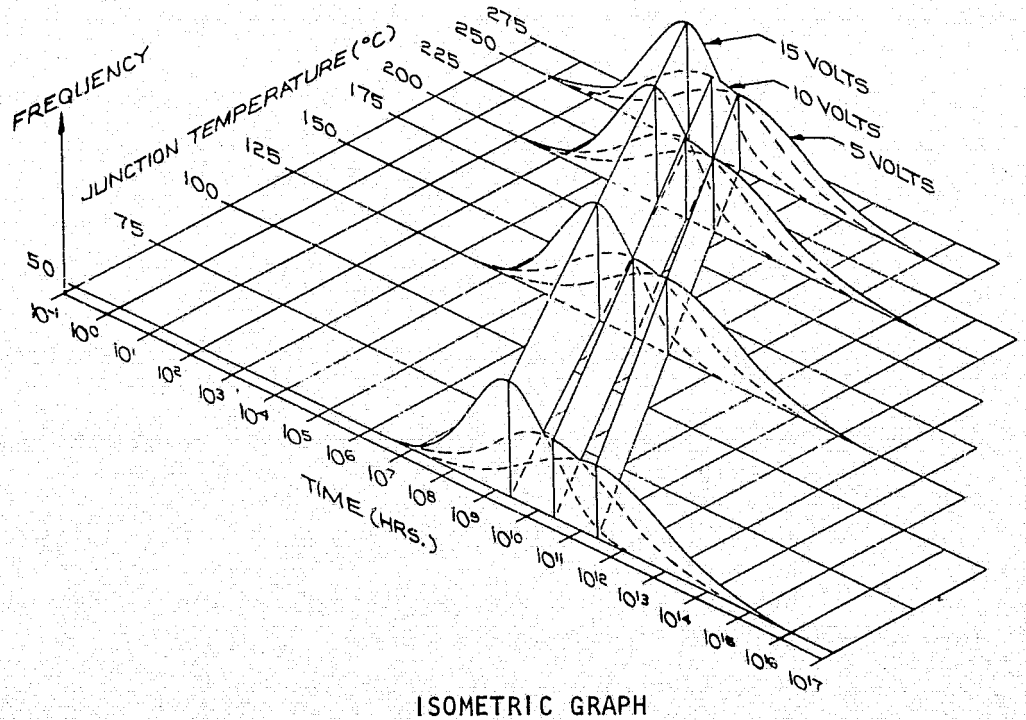
For a bimodal distribution consisting of two lognormal failure rates, the total failure rate is:

$$\lambda(t)_{Total} = \left\{\lambda(t)_{Freak}\right\} (\%\ Freak) + \left\{\lambda(t)_{Main}\right\} (\%\ Main) \qquad (10)$$

Using the median lifetimes, standard deviations and Arrhenius/Eyring model parameters previously defined, failure rates can be computed as a function of time. The results of a computer-aided solution of equations (9) and (10) are presented in Figure 15 for 125°C and 50°C, median lifetimes and standard

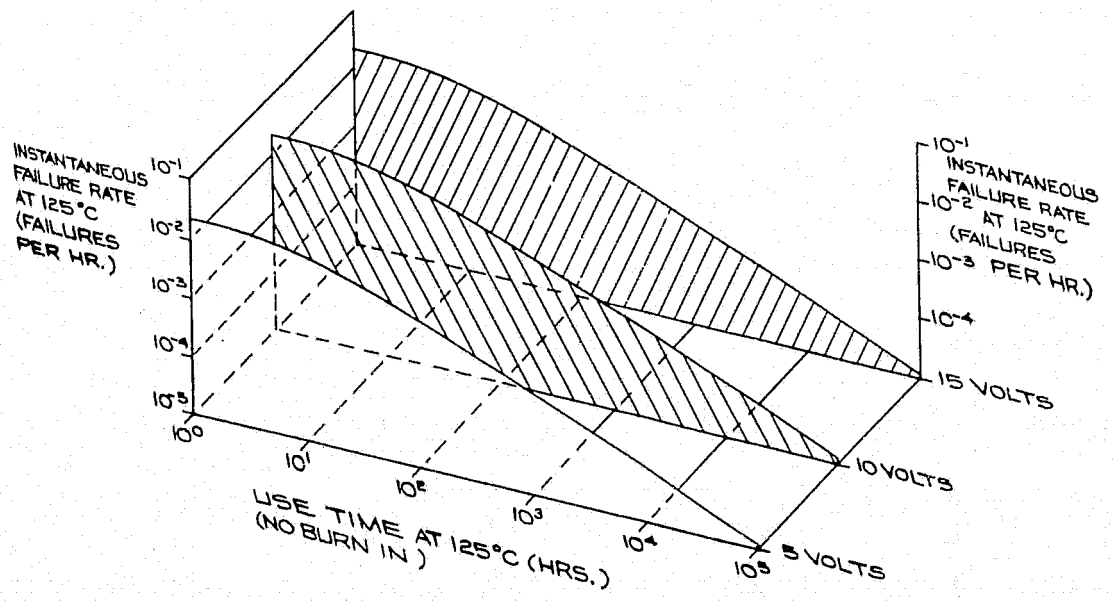


EYRING PLOT

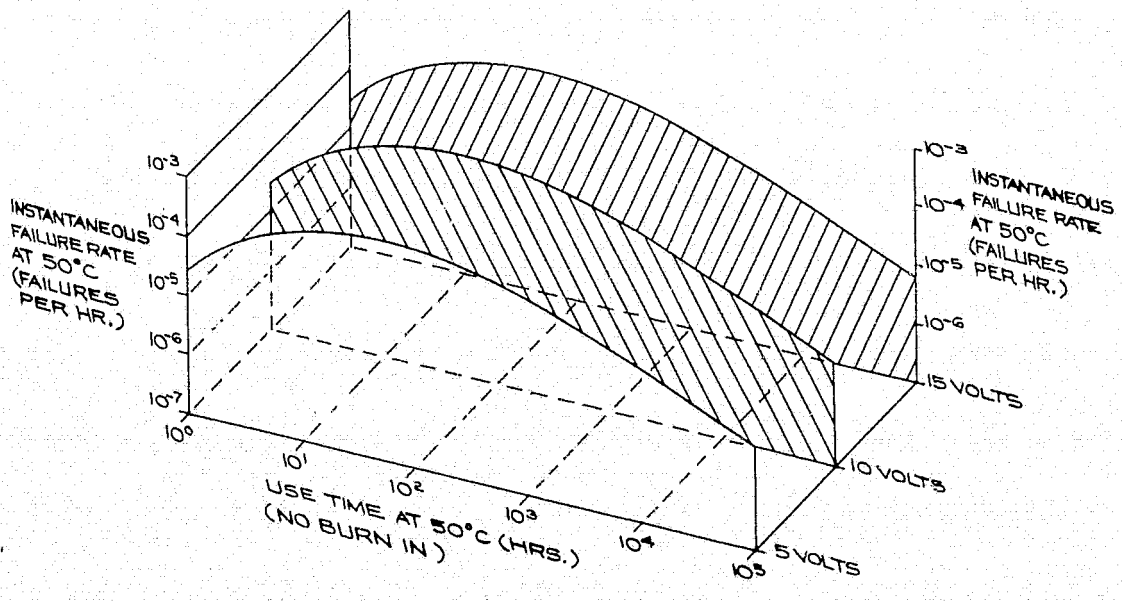


ISOMETRIC GRAPH

FIGURE 14. EYRING PLOT & ISOMETRIC GRAPH, MAIN DISTRIBUTION



125°C FAILURE RATES

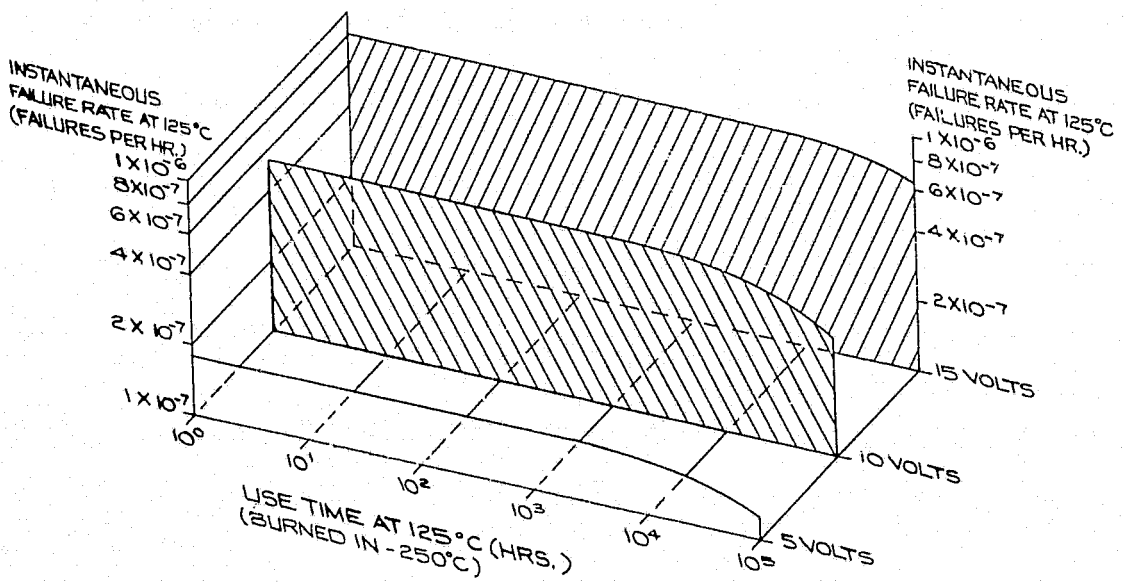


50°C FAILURE RATES

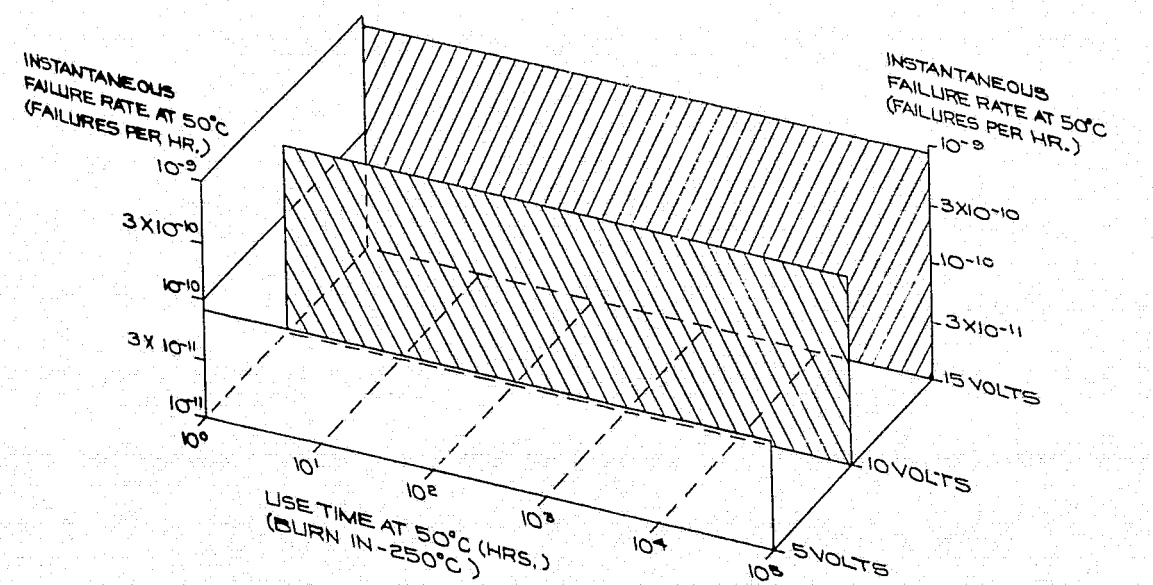
FIGURE 15. INSTANTANEOUS FAILURE RATES - NO BURN-IN

deviations. These results indicate that the nonvoltage dependent "freak" distribution failure rate is the predominant factor in the total failure rate during the first 10^5 hours of use time, and that virtually no failure rate improvement will result from reduced voltage operation during this time period. However, use of a high temperature burn-in to eliminate the "freak" population of devices results in failure rates determined only by the voltage dependent "main" distribution as shown in Figure 16. After elimination of the "freak" population, operation at reduced voltage does result in improved failure rates. An order of magnitude improvement in failure rate is indicated by reducing the operating voltage from 15 volts to 5 volts.

The burn-in time required to remove a percentage of the "freak" population is shown in Figure 17 for several ambient temperatures. Although a 100% probability of complete "freak" removal cannot be achieved in reasonable time, it is sufficient to assume complete "freak" removal at the 99.9% point indicated in Figure 17. Based on this assumption, a 30 hour burn-in at 250°C would constitute complete removal of the "freak" population.



125°C FAILURE RATES



50°C FAILURE RATES

FIGURE 16. INSTANTANEOUS FAILURE RATES AFTER BURN-IN

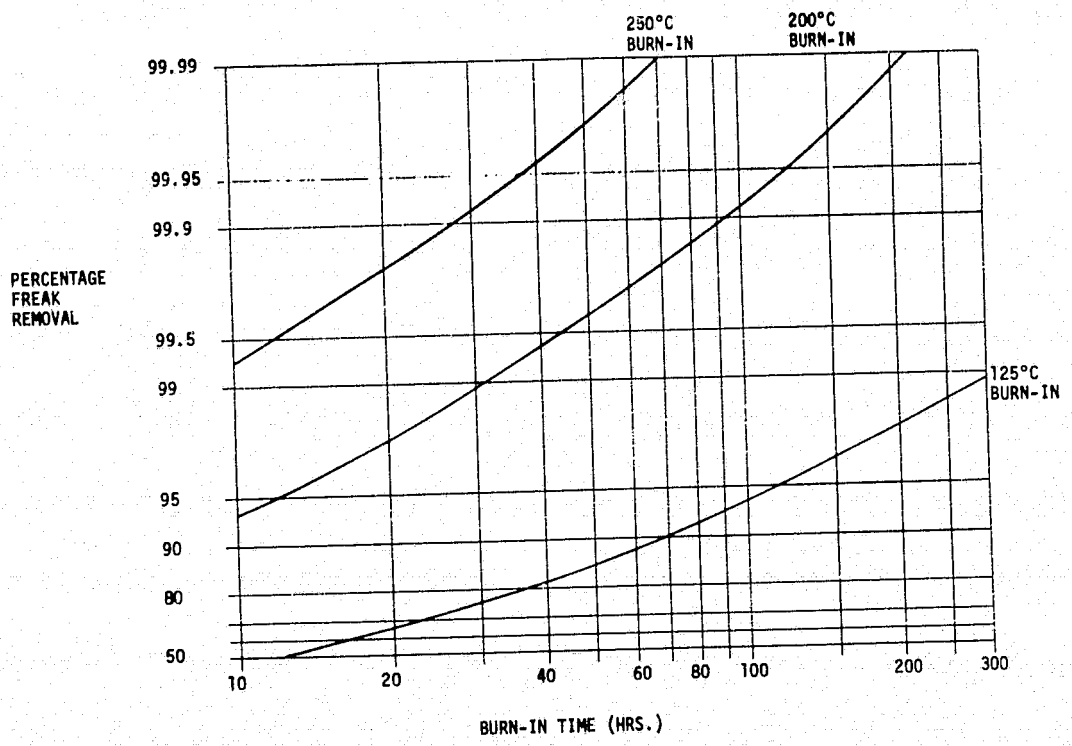


FIGURE 17. BURN-IN TIME & TEMPERATURE FOR FREAK REMOVAL

7.0 CONCLUSIONS & RECOMMENDATIONS

The evaluation of voltage stress effects upon microcircuit failure rates has shown that voltage stress has a definite effect upon failure rates resulting from certain types of surface related failure mechanisms. At 50°C, a reduction of applied voltage from 15 volts to 5 volts results in approximately one order of magnitude improvement in "main" distribution failure rates due to slow hole trapping and cation drift failure mechanisms. Failure rates due to a different type of cation drift observed in the "freak" distribution of failures did not exhibit this voltage dependence. However, the lack of voltage dependence is not conclusive due to the rapid occurrence of failures during the first hour at the accelerated test temperatures. Almost all of the "freak" distribution failures occurred between the zero and one hour measurement points, which precluded an accurate interpolation of actual device failure times.

The Arrhenius reaction rate model provided a good representation of device aging as a function of temperature for both the "freak" and "main" distributions. An Arrhenius model apparent activation energy of 0.52 eV was calculated for the "freak" distribution, and apparent activation energies of 0.99 eV to 1.12 eV were calculated for "main" distributions at voltage conditions between 15 volts and 5 volts, respectively.

The Eyring model appeared to provide a reasonable description of the "main" distribution aging characteristics as a function of both temperature and voltage. However, the lack of a median life point, due to insufficient failure data, at an important/temperature voltage combination, hampered a rigorous evaluation of all the Eyring model parameters. The small number of "main" distribution failures at all the life test conditions also hampered a rigorous determination of the exact nature of the median life versus voltage function. Nevertheless, sufficient information was derived from the matrix of six accelerated life tests to formulate an Eyring model that should provide a reasonable characterization of device aging as a function of temperature and voltages between 5 and 15 volts.

This study has provided valuable insights into the nature of voltage stress effects on microcircuit failure rates. Additional investigations are necessary

to more fully characterize the observed effects in terms of an Eyring reaction rate model, and to evaluate the applicability of the model for a range of device types. It is recommended that additional studies be performed with other CMOS and linear device types from several manufacturers. The matrix of accelerated life tests should also be expanded to include a broader temperature range (125°C to 250°C), and at least three voltage conditions at two of the test temperatures.

8.0 REFERENCES

[1] M. Stitch, G. M. Johnson, B. P. Kirk, and J. B. Brauer, "Microcircuit Accelerated Testing Using High Temperature Operating Tests," IEEE Transactions on Reliability, Vol. R-24, No. 4, pp 238-250, October 1975, and Vol. R-25, No. 1, p. 62, April 1976.

[2] D. S. Peck and C. H. Zierdt, Jr., "The Reliability of Semiconductor Devices in the Bell System," Proceedings of the IEEE, Vol. 62, pp 185-211, February 1974.

[3] F. H. Reynolds, "Thermally Accelerated Aging of Semiconductor Components," Proceedings of IEEE, Vol. 62, pp 212-222, February 1974.

[4] J. Vaccaro and H. C. Gorton, "RADC Reliability Physics Notebook," RADC-TR-65-330, Sections 1 and 4, November 19, 1965.

[5] D. S. Peck, "The Analysis of Data from Accelerated Stress Tests," Proceedings 9th Annual Reliability Physics Symp., pp 68-83, 1971.

[6] M. G. Natrella, "Experimental Statistics," National Bureau of Standards Handbook 91, August 1963.

[7] E. H. Snow, A. S. Grove, B. E. Deal, and C. T. Sah, "Ion Transport Phenomenon in Insulating Films," Journal of Applied Physics, Volume 36, No. 5, pp 1664-1673, May 1965.

[8] Keith J. Laidler, "Reaction Kinetics," Volume I, p 87, Pergamon Press, New York, 1970.

[9] Lynn R. Goldthwaite, "Failure Rate Study for the Log Normal Lifetime Model," IRE (NSRQCE) Conference, pp 208-213, 1961.

APPENDIX A

ELECTRICAL TEST CONDITIONS

TABLE A1 - LOT A

TABLE A2 - LOT B

TABLE A1. ELECTRICAL TEST CONDITIONS - LOT A

SYMBOL	MIL-STD-883 METHOD	TEST NO.	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN) (SEE NOTE G)														MEAS. TERMINAL	TEST LIMITS T_A = 25°C		UNITS
			1	2	3	4	5	6	7	8	9	10	11	12	13	14		MIN	MAX	
			2aY	2aS	2A	2bS	2bY	1A	V_{SS}	1bY	3bS	3A	3aS	3Y	1aY	V_{DD}				
I_{IL}	3009	1	(5)	15V	GND	GND	(1)	GND	GND	(13)	GND	GND	15V		(8)	15V	1A		10.0*	nA
I_{IL}	3009	2	(5)	15V	GND	GND	(1)	GND	GND	(13)	GND	GND	15V		(8)	15V	2A		10.0*	nA
I_{IL}	3009	3	(5)	15V	GND	GND	(1)	GND	GND	(13)	GND	GND	15V		(8)	15V	3A		10.0*	nA
I_{IH}	3010	4	(5)	GND	GND	-15V	(1)	GND	-15V	(13)	-15V	GND	GND		(8)	GND	1A to V_{DD}		10.0*	nA
I_{IH}	3010	5	(5)	GND	GND	-15V	(1)	GND	-15V	(13)	-15V	GND	GND		(8)	GND	2A to V_{DD}		10.0*	nA
I_{IH}	3010	6	(5)	GND	GND	-15V	(1)	GND	-15V	(13)	-15V	GND	GND		(8)	GND	3A to V_{DD}		10.0*	nA
V_{OL1}	3007	7	(5)	5.0V	GND	GND	(1)	4.5V	GND	(13)	GND	GND	5.0V		(8)A	5.0V	1aY		0.4	Vdc
V_{OL1}	3007	8	(5)A	5.0V	4.5V	GND	(1)	GND	GND	(13)	GND	GND	5.0V		(8)	5.0V	2aY		0.4	Vdc
V_{OL1}	3007	9	(5)	5.0V	GND	GND	(1)	GND	GND	(13)	GND	4.5V	5.0V	A	(8)	5.0V	3Y		0.4	Vdc
V_{OL2}	3007	10	(5)	15V	GND	GND	(1)	14.5V	GND	(13)	GND	GND	15V		(8)	15V	1aY		10	mVdc
V_{OL2}	3007	11	(5)	15V	14.5V	GND	(1)	GND	GND	(13)	GND	GND	15V		(8)	15V	2aY		10	mVdc
V_{OL2}	3007	12	(5)	15V	GND	GND	(1)	GND	GND	(13)	GND	14.5V	15V		(8)	15V	3Y		10	mVdc
V_{OH1}	3006	13	(5)	5.0V	GND	GND	(1)	0.5V	GND	(13)	GND	GND	5.0V		(8)B	5.0V	1aY	3.6		Vdc
V_{OH1}	3006	14	(5)B	5.0V	0.5V	GND	(1)	GND	GND	(13)	GND	GND	5.0V		(8)	5.0V	2aY	3.6		Vdc
V_{OH1}	3006	15	(5)	5.0V	GND	GND	(1)	GND	GND	(13)	GND	0.5V	5.0V	B	(6)	5.0V	3Y	3.6		Vdc
V_{OH2}	3006	16	(5)	15V	GND	GND	(1)	0.5V	GND	(13)	GND	GND	15V		(8)	15V	V_{DD} to 1aY		10	mVdc
V_{OH2}	3006	17	(5)	15V	0.5V	GND	(1)	GND	GND	(13)	GND	GND	15V		(8)	15V	V_{DD} to 2aY		10	mVdc
V_{OH2}	3006	18	(5)	15V	GND	GND	(1)	GND	GND	(13)	GND	0.5V	15V		(8)	15V	V_{DD} to 3Y		10	mVdc
V_{03}	3006	19	(5)	5.0V	GND	GND	(1)	C	GND	(13)	GND	GND	5.0V		(8)	5.0V	V_{DD} to 1aY		10	mVdc
V_{03}	3006	20	(5)	5.0V	C	GND	(1)	GND	GND	(13)	GND	GND	5.0V		(8)	5.0V	V_{DD} to 2aY		10	mVdc
V_{03}	3006	21	(5)	5.0V	GND	GND	(1)	GND	GND	(13)	GND	C	5.0V		(8)	5.0V	V_{DD} to 3Y		10	mVdc
V_{06}	3006	28	(5)	5.0V	GND	GND	(1)	F	GND	(13)	GND	GND	5.0V		(8)	5.0V	1aY		0.1	Vdc
V_{06}	3006	29	(5)	5.0V	F	GND	(1)	GND	GND	(13)	GND	GND	5.0V		(8)	5.0V	2aY		0.1	Vdc
V_{06}	3006	30	(5)	5.0V	GND	GND	(1)	GND	GND	(13)	GND	F	5.0V		(8)	5.0V	3Y		0.1	Vdc
I_{SS}	3005	31	(5)	15V	GND	GND	(1)	GND	GND	(13)	GND	GND	15V		(8)	15V	V_{SS}		50	nA
I_{SS}	3005	32	(5)	15V	15V	GND	(1)	15V	GND	(13)	GND	15V	15V		(8)	15V	V_{SS}		50	nA

NOTES:
A. I_{OL} = 600µA
B. I_{OH} = -0.75 mA
C. V_{13} = 1.1V
D. V_{14} = 2.7V
E. V_{15} = 2.0V
F. V_{16} = 3.8V
G. Terminals in parentheses are connected together as indicated by the included number.
H. ASTERIK (*) denotes departure from M38510/05301 (NASA).

TABLE A2. ELECTRICAL TEST CONDITIONS - LOT B

SYMBOL	MIL-STD-883 METHOD	CASE A,C,D TEST NO.	TERMINAL CONDITIONS AND LIMITS																LIMITS SUBGROUP 1 TA = 25°C		UNITS
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	MEAS. TERMINAL		MIN	MAX	
			2aY	2as	2A	2bs	2bY	1A	V_{SS}	1bY	3bs	3A	3as	3Y	1aY	V_{DD}					
V_{IC} (POS)		1	(5)	GND			(5)	1 mA		(13)			GND		(8)	GND	1A			1.5	Vdc
V_{IC} (POS)		2		GND	1 mA								GND			GND	2A			1.5	
V_{IC} (POS)		3		GND								1 mA	GND			GND	3A			1.5	
V_{IC} (NEG)		4				GND		-1 mA	GND		GND						1A			-.6	
V_{IC} (NEG)		5			-1 mA												2A			-.6	
V_{IC} (NEG)		6										-1 mA					3A			-.6	
I_{SS}	3005	7		15 V	GND			GND				GND	15 V			15 V	2bs, V_{SS}, 3bs*			-50	nA
I_{SS}	3005	8		15 V	15 V			15 V				15 V	15 V			15 V	2bs, V_{SS}, 3bs*			-50	nA
V_{OH1}	3006	9		4.5 V	GND			V_{IL1}				GND	4.5 V		I_{OH1}	4.5 V	1aY	2.5			Vdc
V_{OH1}		10	I_{OH1}	4.5 V	V_{IL1}			GND				GND	4.5 V			4.5 V	2aY	2.5			
V_{OH1}		11		4.5 V	GND			GND				V_{IL1}	4.5 V	I_{OH1}		4.5 V	3Y	2.5			
V_{OH2}		12		5.0 V	GND			V_{IL1}				GND	5.0 V		I_{OH2}	5.0V	1aY	4.0*			
V_{OH2}		13	I_{OH2}		V_{IL1}			GND				GND					2aY	4.0*			
V_{OH2}		14			GND			GND				V_{IL1}		I_{OH2}			3Y	4.0*			
V_{OH3}		15			GND			V_{IL1}				GND					1aY	4.95			
V_{OH3}		16			V_{IL1}			GND				GND					2aY	4.95			
V_{OH3}		17			GND			GND				V_{IL1}					3Y	4.95			
V_{OH4}		18		12.5 V	GND			V_{IL2}				GND	12.5 V			12.5 V	1aY	11.25			
V_{OH4}		19		12.5 V	V_{IL2}			GND				GND	12.5 V			12.5 V	2aY	11.25			
V_{OH4}		20		12.5 V	GND			GND				V_{IL2}	12.5 V			12.5 V	3Y	11.25			
V_{OL1}	3007	21		5.5 V	GND			V_{IH1}				GND	5.5 V		I_{OL1}	5.5 V	1aY		0.4		
V_{OL1}		22	I_{OL1}	5.5 V	V_{IH1}			GND				GND	5.5 V			5.5 V	2aY		0.4		
V_{OL1}		23		5.5 V	GND			GND				V_{IH1}	5.5 V	I_{OL1}		5.5 V	3Y		.0.4		
V_{OL2}		24		5.0 V	GND			V_{IH1}				GND	5.0 V		I_{OL2}	5.0 V	1aY		0.6*		
V_{OL2}		25	I_{OL2}		V_{IH1}			GND				GND					2aY		0.6*		
V_{OL2}		26			GND			GND				V_{IH1}		I_{OL2}			3Y		0.6*		
V_{OL3}		27			GND			V_{IH1}				GND					1aY		50	mVdc	
V_{OL3}		28			V_{IH1}			GND				GND					2aY		50	mVdc	
V_{OL3}		29			GND			GND				V_{IH1}					3Y		50	mVdc	
V_{OL4}		30		12.5 V	GND			V_{IH2}				GND	12.5 V			12.5 V	1aY		1.25	Vdc	
V_{OL4}		31		12.5 V	V_{IH2}			GND				GND	12.5 V			12.5 V	2aY		1.25	Vdc	
V_{OL4}		32		12.5 V	GND			GND				V_{IH2}	12.5 V			12.5 V	3Y		1.25	Vdc	
I_{IH1}		33		15 V	15 V			15 V				15 V	15 V			15 V	ALL INPUTS TOGETHER		10.0*	nA	
I_{IL1}	3009	34		15 V	GND			GND				GND	15 V			15 V	ALL INPUTS TOGETHER		-10.0*	nA	

NOTES:

A. PINS NOT DESIGNATED MAY BE "HIGH" LEVEL LOGIC, "LOW" LEVEL LOGIC OR OPEN.
B. I_{OH1} = -0.1 mA AT 25°C
C. I_{OH2} = -0.75 mA AT 25°C
D. V_{IH1} = 3.8 V AT 25°C
E. V_{IH2} = 9.5 V AT 25°C
F. I_{OL1} = 0.23 mA AT 25°C
G. I_{OL2} = 600 µ A AT 25°C
H. V_{IL1} = 1.1 V AT 25°C
I. V_{IL2} = 2.8 V AT 25°C
J. TERMINALS IN PARENTHESES ARE CONNECTED TOGETHER AS INDICATED BY THE INCLUDED NUMBER.
K. ASTERISK (*) DENOTES DEPARTURE FROM M38510/05301 (REV. A)

APPENDIX B

MICROCIRCUIT CONSTRUCTION ANALYSES

CMOS 4007 - DUAL COMPLEMENTARY PAIR

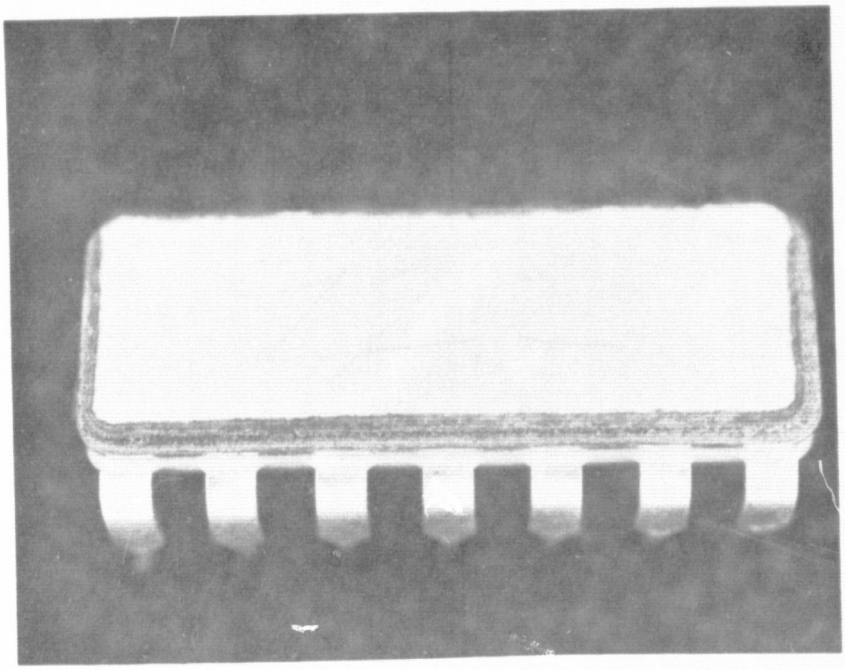
PLUS INVERTER

APPENDIX B1 - LOT A

APPENDIX B2 - LOT B

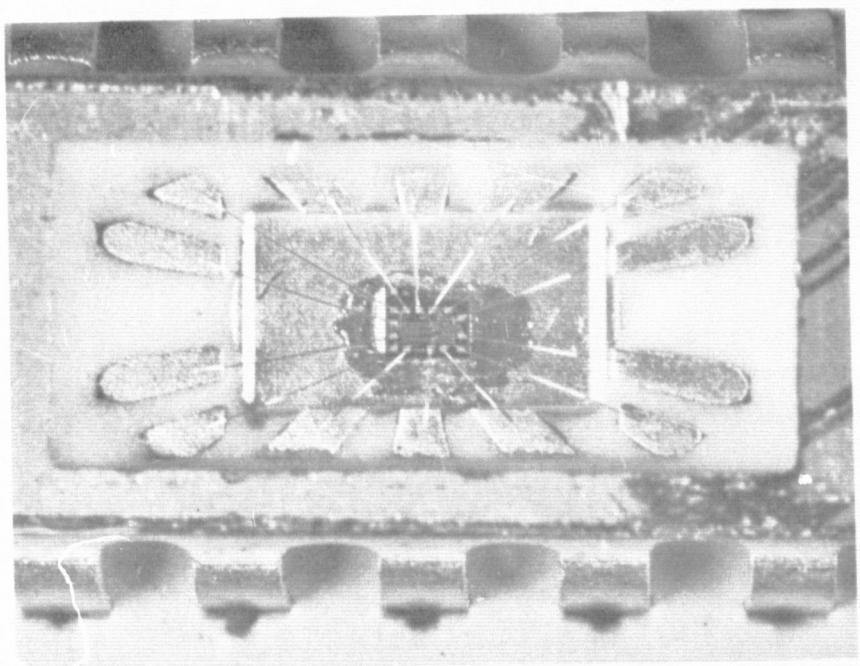
APPENDIX B1 - LOT A

1. IDENTIFICATION
   a. Part Name: Dual Complementary Pair Plus Inverter
   b. Part Number: M38510/053-01
   c. Date Code: None
   d. Package Type: Ceramic Dual In-Line with Metal Lid
2. PACKAGE CONDITION
   a. Cracks, chips, etc.: No cracks or chips
   b. Hermeticity: Gross Leak acceptable. Fine leak 2.1 X 10^{-8} attm cc/sec
3. PACKAGE CONSTRUCTION - Figure B1
   a. Material & Dimensions: Kovar and Glass, 1/4 X 3/4 inches
   b. Lid Seal: Solder
   c. Lead Type, material and plating: Gold plated Kovar
4. INTERNAL VISUAL EXAMINATION - Figure B2
   a. Contamination: Surface of die is relatively clean
   b. Metallization: Aluminum
   c. Pad Size: 13 - (square .0040"), 1 = (hexagonal .0050" x .0040" x .0049")
   d. Surface Protection: Glassivation
   e. Chip mount: Eutectic
   f. Lead Frame: Gold Plated Kovar
   g. Wire: .0012" Aluminum
   h. Bond at chip: Figure B3 - Ultrasonic Bond
   i. Bond at post: Figure B4 - Ultrasonic Bond
   j. Chip dimension: .038" X .025" - Figure B5
   k. General condition: Good
      1) The geometry of the die is shown in Figure B6.
5. SCHEMATIC DIAGRAM - Figure B7



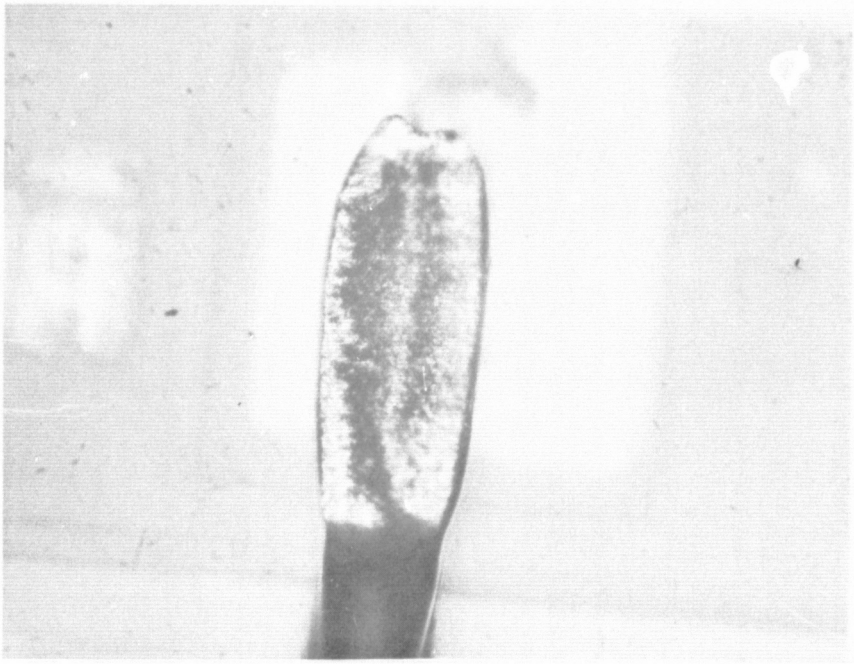
5X

FIGURE NO. B1 - EXTERNAL PACKAGE



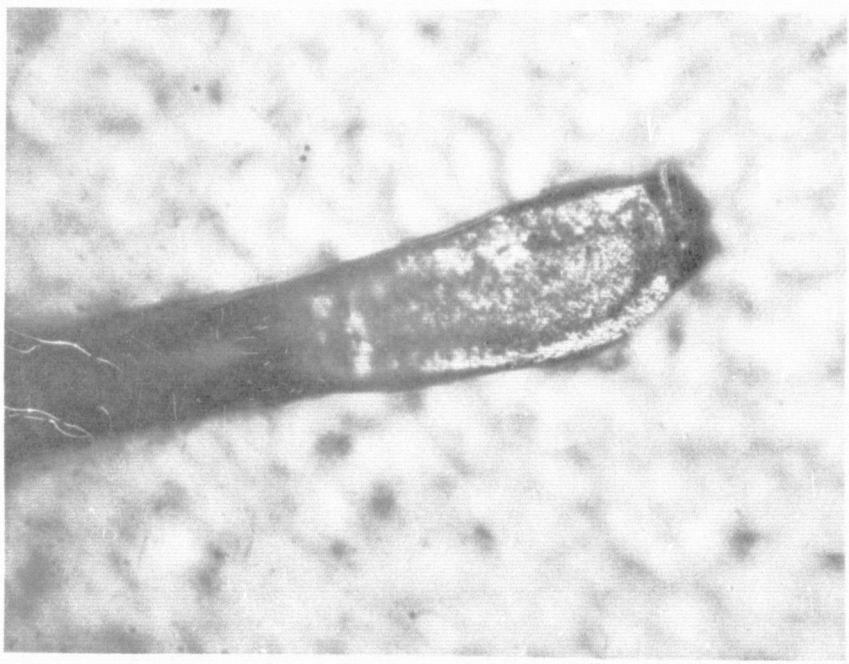
10X

FIGURE NO. B2 - INTERNAL CAVITY



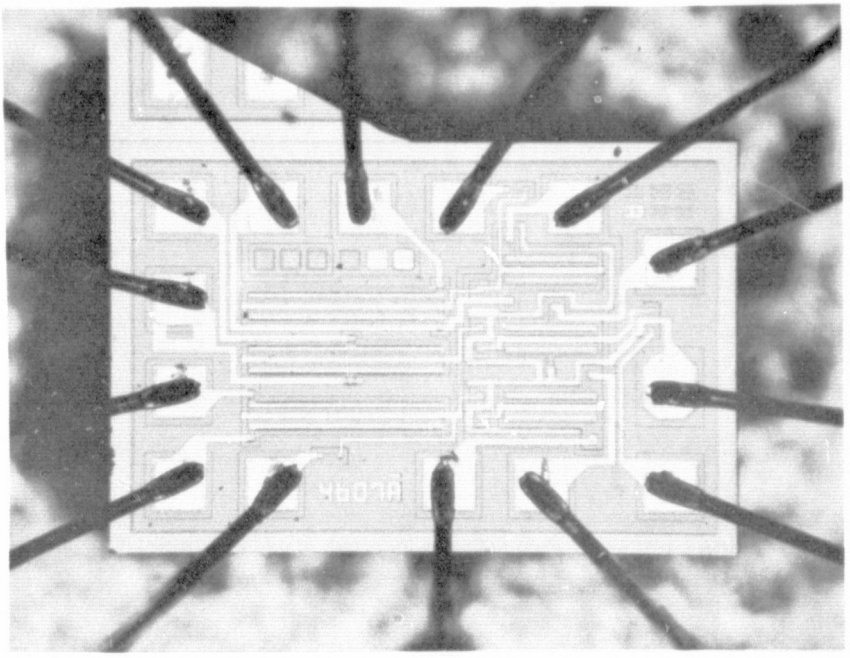
491X

FIGURE NO. B3 - BOND AT CHIP



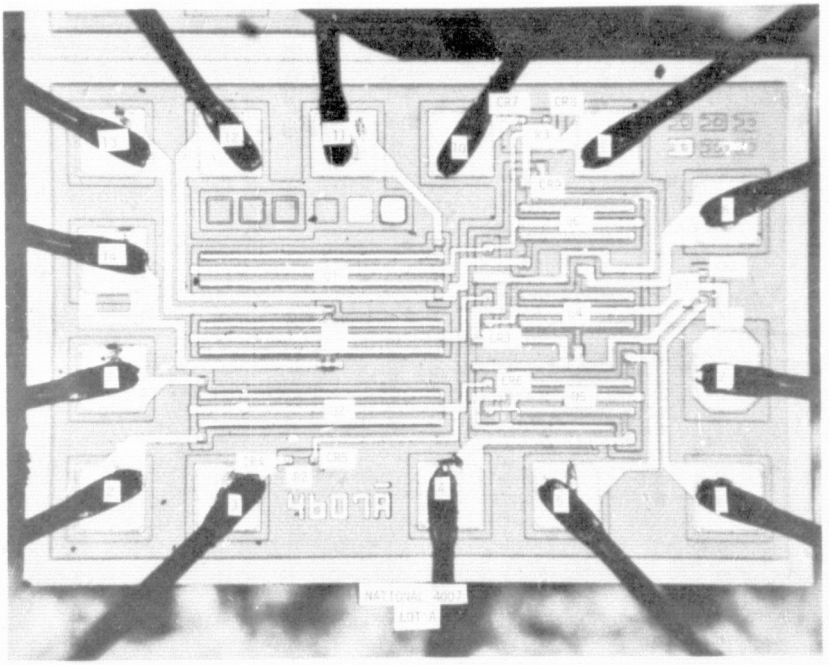
491X

FIGURE NO. B4 - BOND AT POST



85X

FIGURE NO. B5 - DIE PHOTO



110X

FIGURE NO. B6 - CHIP GEOMETRY

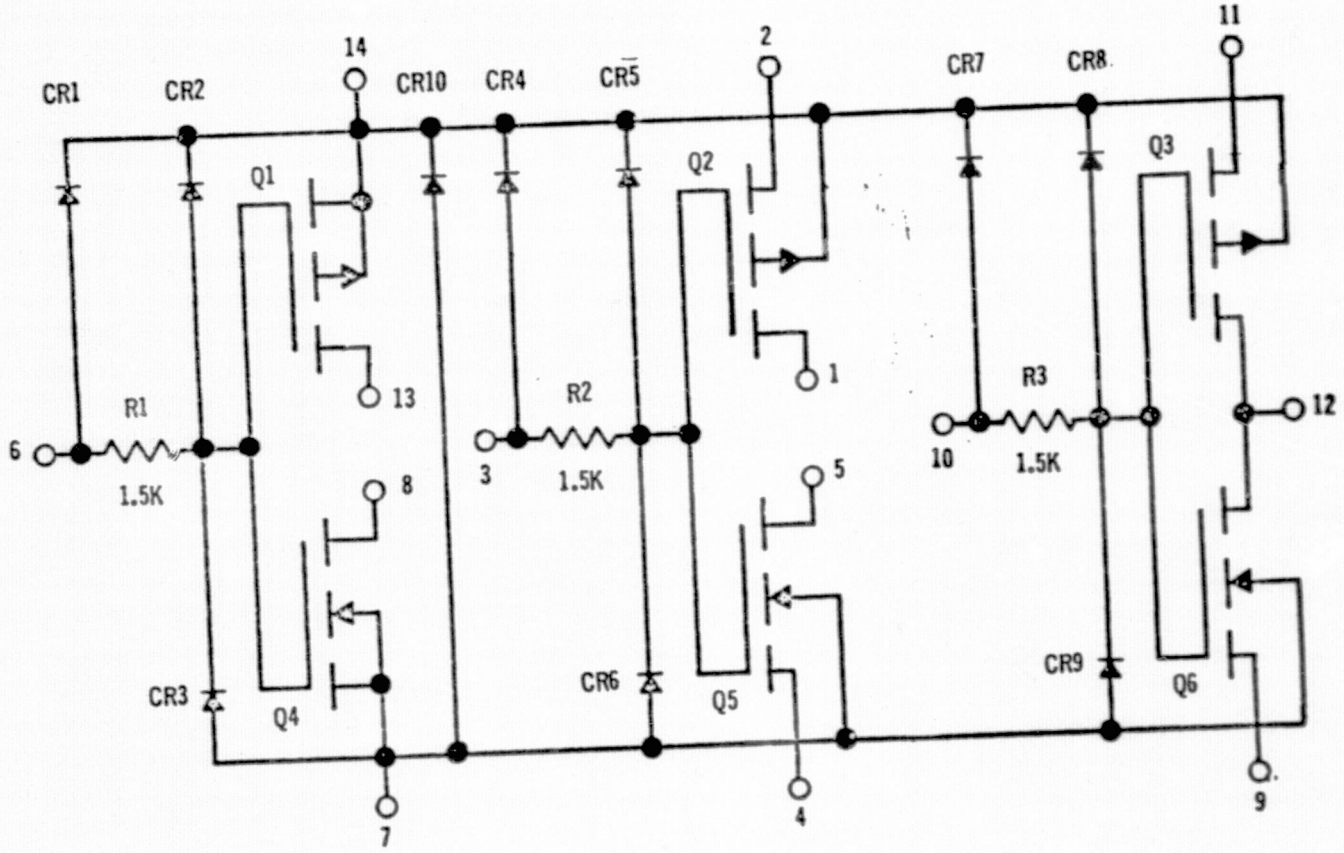


FIGURE NO. B7 - SCHEMATIC

APPENDIX B2 - LOT B

1. IDENTIFICATION
   a. Part Name: Dual Complementary Pair Plus Inverter
   b. Part Number: M38510/05301 (MM4607AD CD4007AD)
   c. Date Code: 525
   d. Package Type: Dual In-Line Ceramic with Metal Lid
2. PACKAGE CONDITION
   a. Cracks, chips, etc.: No cracks or chips. Solder splashes on lid later shown to have not affected interior.
3. PACKAGE CONSTRUCTION - Figure B8
   a. Material & Dimensions: Ceramic with metal lid 1/4" x 3/4"
   b. Lid Seal: Solder
   c. Lead Type, Material and Plating: Gold-Plated Kovar Leads Braze Welded to Package
4. INTERNAL VISUAL EXAMINATION - Figure B9
   a. Contamination: Cavity reasonably clean
   b. Metallization: Aluminum
   c. Pad Size: Square - 0.004", Hex - 0.005" X 0.004" X .0049"
   d. Surface Protection: Glassivation
   e. Chip Mount: Eutectic
   f. Lead Frame: Gold Thin Film
   g. Wire: Aluminum - .0012 inch
   h. Bond at Chip: Al-Al Ultrasonic - Figure B10 and B11
   i. Bond at Frame: Al-Au Ultrasonic - Figure B12 and B13
   j. Chip Dimension: 0.038 x 0.025 inch - Figure B14
   k. General Condition:
      1) The geometry of the die, Figure B15, is exactly the same as the geometry used in the first lot of devices.
      2) As was the case in the first lot of devices, this device has the problem of insufficient clearance between the interconnect wires and the edge of the die, Figure B16 and B17, due to 1) placement of the bond pads relatively close to the scribe area, 2) misplacement of the bond toward the scribe area (Figure B14), and 3) shallow angles

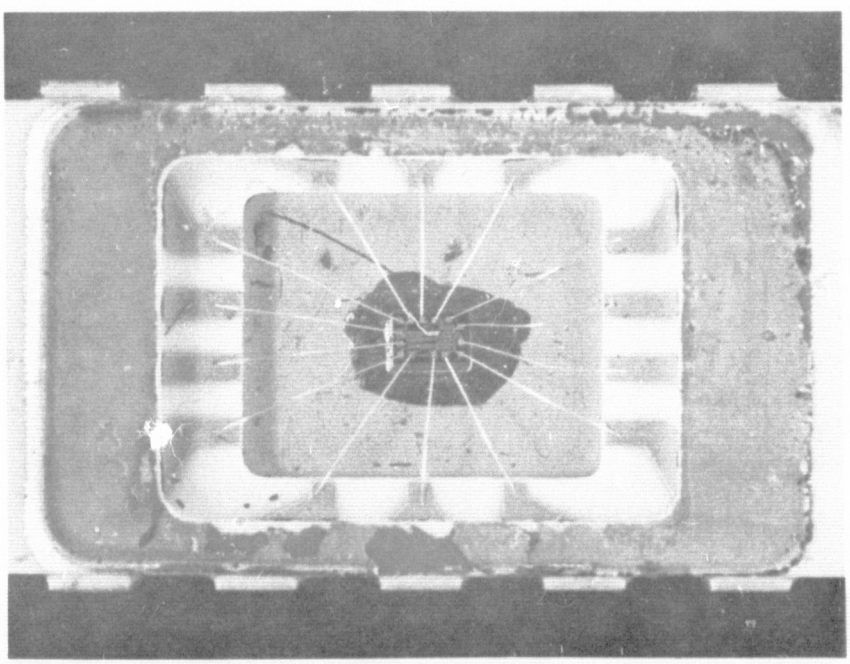
k. General Condition: (Continued)

due to long lead length, low profile cavity and the use of ultrasonically bonded aluminum wire.

5. SCHEMATIC DIAGRAM - Figure B18

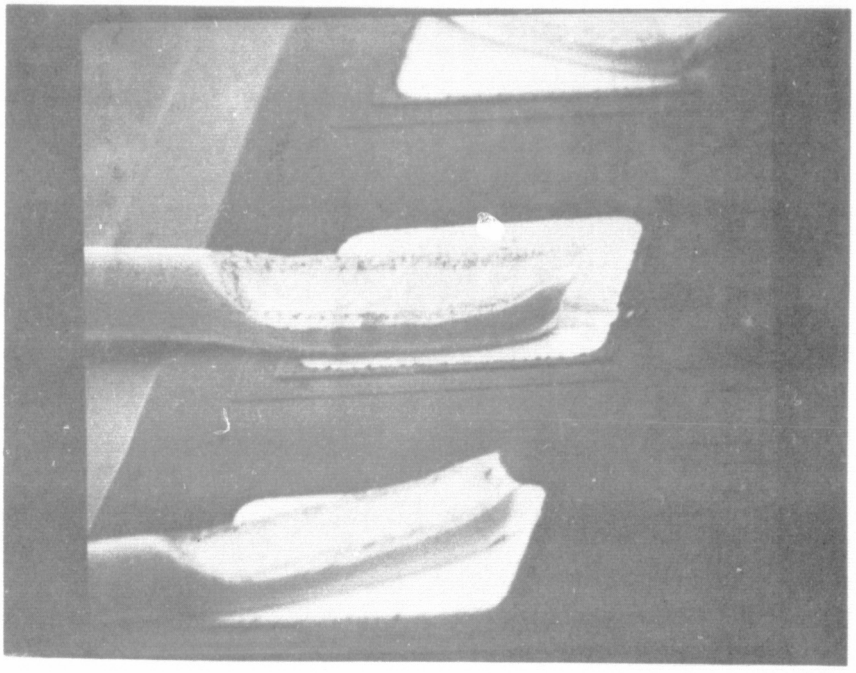
4X

FIGURE NO. B8 - EXTERNAL PACKAGE



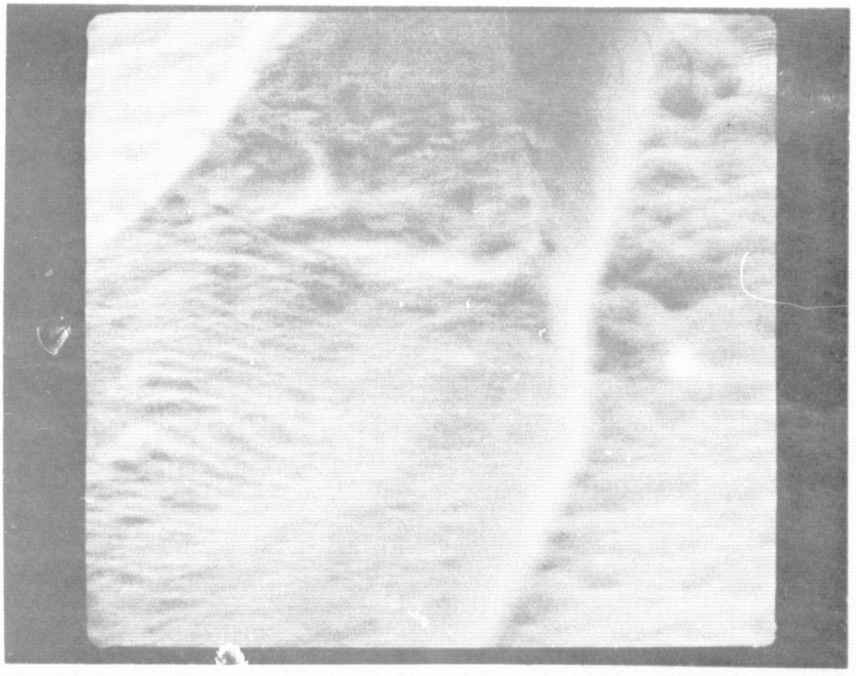
10X

FIGURE NO. B9 - INTERNAL GEOMETRY



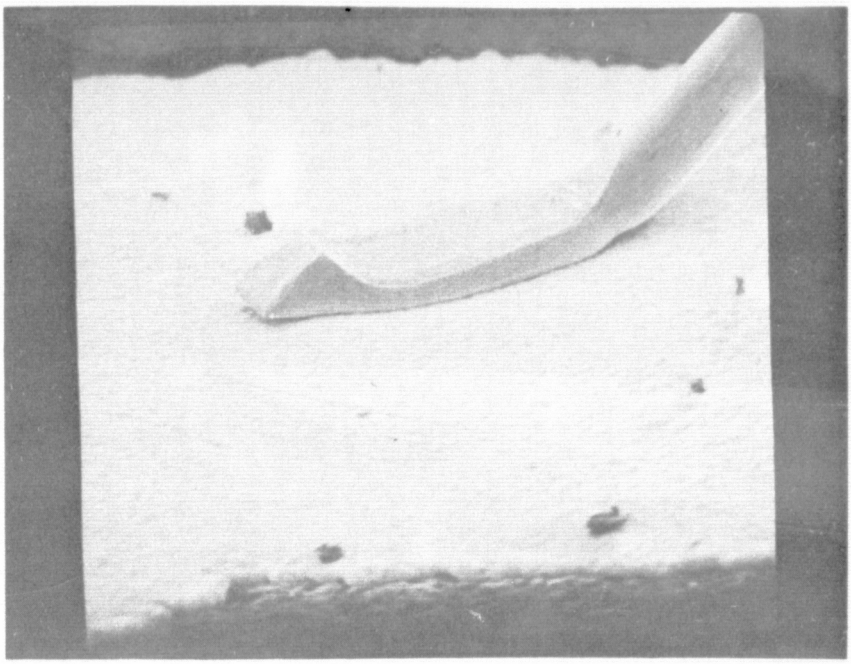
625X

FIGURE NO. B10 - WIRE BOND AT THE CHIP (TYPICAL)



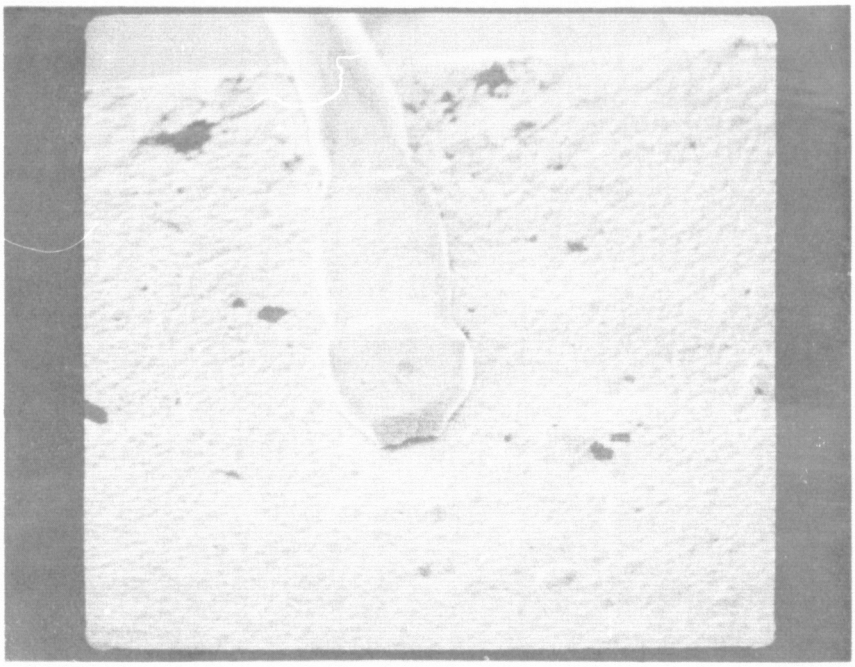
1750X

FIGURE NO. B11 - DIE PAD BOND



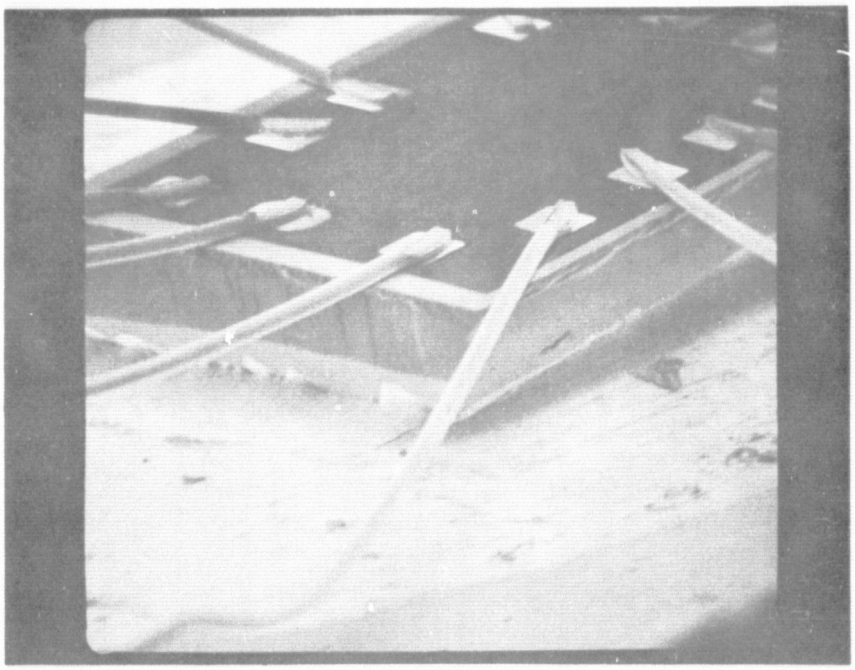
475X

FIGURE NO. B12 - WIRE BOND AT LEAD FRAME (TYPICAL)



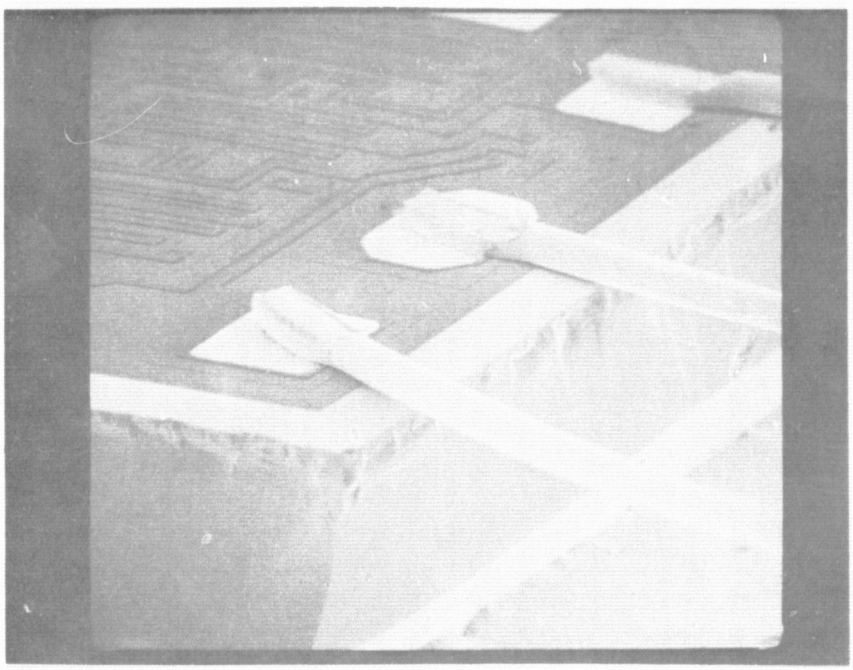
625X

FIGURE NO. B13 - WIRE BOND AT LEAD FRAME (NOT TYPICAL)



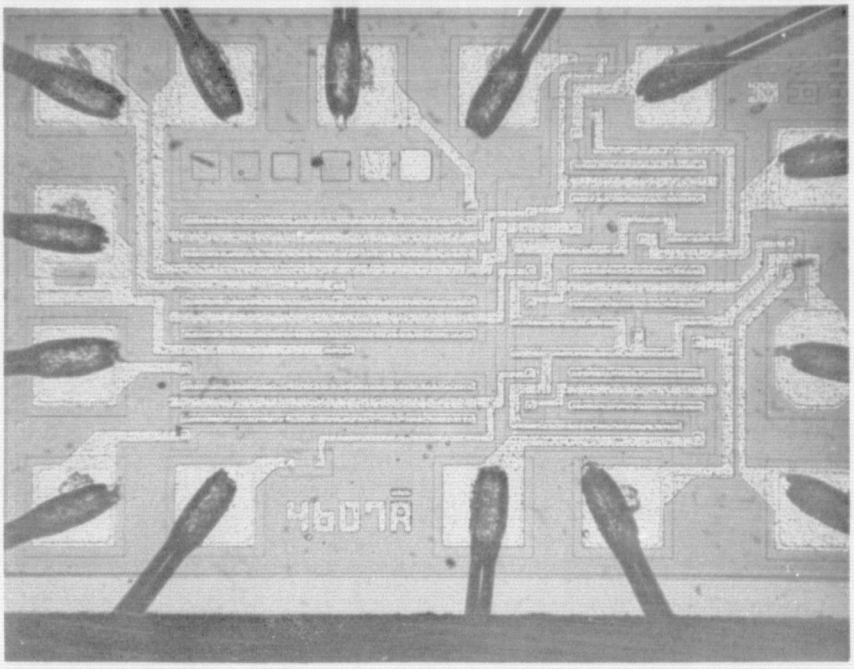
100X

FIGURE NO. B14 - POOR WIRE TO SCRIBE AREA CLEARANCE



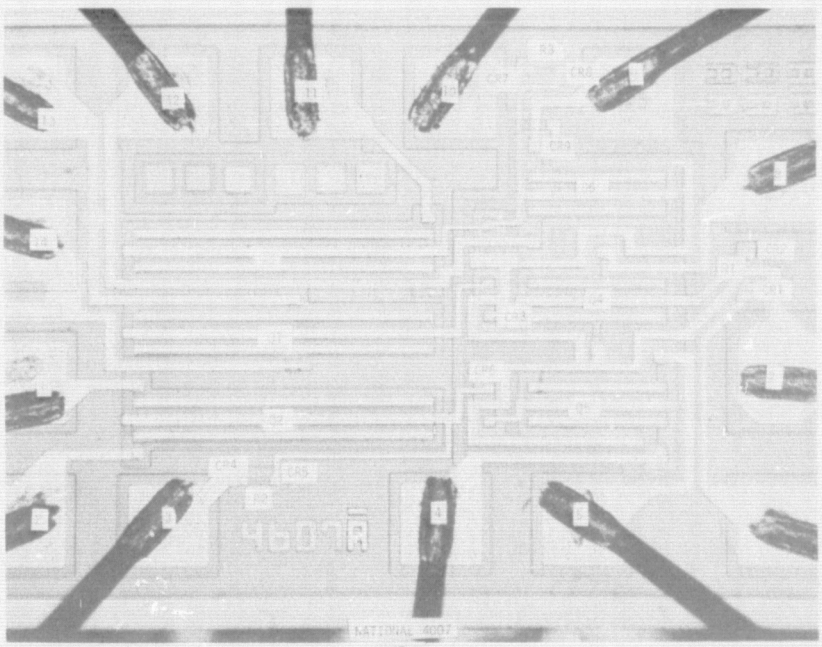
475X

FIGURE NO. B15 - INSUFFICIENT WIRE TO SCRIBE AREA CLEARANCE



105X

FIGURE NO. B16 - PHOTOMICROGRAPH OF THE CHIP



105X

FIGURE NO. B17 - CHIP GEOMETRY

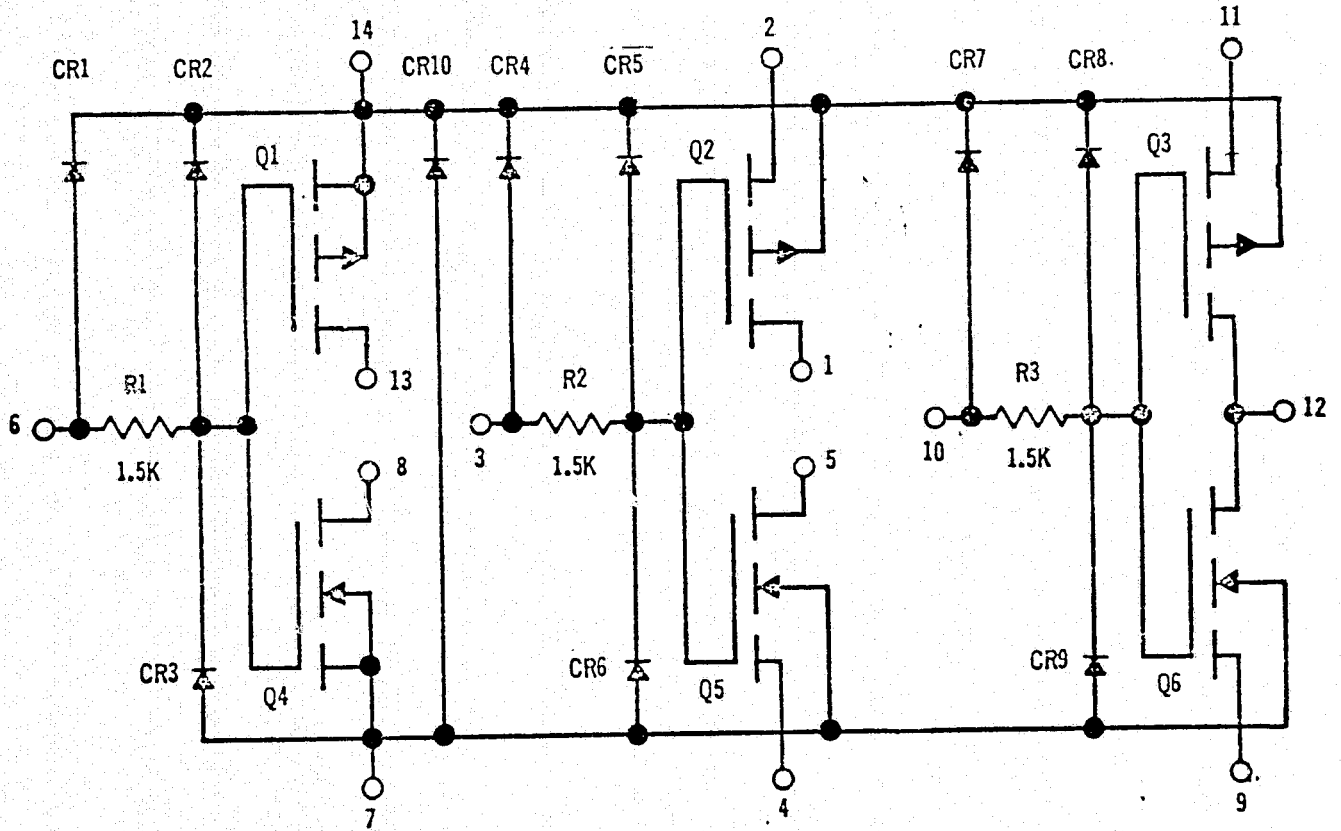


FIGURE NO. B18 - SCHEMATIC

APPENDIX C
FAILURE ANALYSIS

TABLE OF CONTENTS

1.0 PROCEDURE

All microcircuits that failed an electrical test during Step Stress or Life Test were analyzed to determine the particular failure mode, failure mechanism, and probable cause of failure. The general analysis procedure was as follows:

1) All failures were retested separately on the automatic test set to verify the failure.
2) All failed parameters were confirmed using a curve tracer.
3) The failure was isolated to a specific junction or element to the extent possible via external pin-to-pin curve tracer measurements.
4) The failures were classified into subgroups related to failure categories, on the basis of the analysis findings to this point.
5) A representative sample of devices from each subgroup was subjected to detailed analysis, including as a minimum, external optical examination, delidding, internal optical and SEM examinations, die level probing, and chemical or metallurgical dissectioning. Die level probing of defective junctions or components included stripe severing to isolate the degradation to the exact responsible active, parasitic, or spurious element. After this, the specific approach varied depending on the nature of the degradation. If sufficient samples were available, surface instability related failures were sequentially baked, cleaned, or stripped of their passivating layers. Bulk related failures were chemically or metallurgically dissectioned.
6) The remaining samples from each subgroup were subjected to the following steps to confirm their initial classification and to obtain any additional information:
   a) Unpowered Bake - Each device was baked, then retested at 25°C. The exact time and temperature of the bake depended on the time and temperature at which the failure occurred. Usually, an overnight bake (16 hours) at the test cell temperature sufficed. In most instances, no attempt was made to obtain any quantitative information from these bakes other than whether or not the device cured or improved sufficiently to establish that a surface-related mechanism existed.

b) Leak Tests - Each device was subjected to a helium bomb fine leak test and a fluorocarbon gross leak test. Unless otherwise stated in the report, the devices did not exhibit any loss of hermeticity.

c) Delidding - Each device was delidded and subjected to routine optical examinations and documentations.

2.0 ANALYSIS SUMMARY

The results of the detailed analyses of the test program failures are summarized in Table C1. The table contains a delineation of the failure symptoms, mode, mechanism, and cause for each failure category.

Detailed reports of each type of failure are presented as referenced in the summary table (Table C1). Failure category numbers referenced in the reports are as defined in the summary table. Parameter symbols, circuit symbols, device pin numbers, etc., referenced in the reports are as previously defined in Appendices A and B; for example, I_{SS} [31] defines quiescent supply current-outputs high, which is test 31.

TABLE C1. SUMMARY OF FAILURE ANALYSIS FINDINGS

FAILURE CATEGORY NUMBER	FAILED PARAMETER(S) OR SYMPTOMS	FAILURE MODE	FAILURE MECHANISM	CAUSE OF FAILURE	QTY. OF FAILURES		F.A. REFERENCES	
					LOT A	LOT B	PARA. NO.	FIGURE NOS.
MECHANICAL AND BULK FAILURES								
1	PIN SHORTED TO V_{DD}	WIRE-TO-DIE SHORT	SAGGING OF THE Al WIRE AND Al-Si ALLOYING	INSUFFICIENT CLEARANCE BETWEEN THE WIRE AND THE EDGE OF THE DIE DUE TO DESIGN AND WORKMANSHIP	17	16	3.1.1	C1-C4
2	A. EXCESSIVE PIN-PIN LEAKAGE CURRENTS - OR - B. OPEN PINS - OR - C. o HIGH I_{SS} [31] o HIGH V_{O3} AND V_{OH2} o LOW V_{OH1}	A. CONDUCTION THROUGH MOISTURE PATHS B. OPEN Al-Au WIRE BONDS C. LOW V_{TH}, Q4, Q5, AND/OR Q6.	A. MOISTURE CONDENSATION DURING COOL-DOWN. B. CORROSION OF THE Al WIRE C. ION DRIFT THROUGH THE GATE OXIDE	CRACKING OF THE GLASS SEAL DURING THERMAL EXCURSIONS WHICH ALLOWED MOISTURE TO ENTER THE PACKAGE.	121	0	3.1.2	C5-C6
3	A. HIGH V_{OL2} [24] - AND/OR - B. LOW V_{OH2} [12]	A. HIGH $V_{DS(ON)}$, Q4 B. HIGH $V_{DS(ON)}$, Q1	INCREASE IN THE SOURCE OHMIC CONTACT RESISTANCE DUE TO SILICON DISSOLUTION	MANUFACTURING ALLOY CYCLE	0	16	3.1.3	C7-C12
4	OPEN PIN	LIFTED Al-Au WIRE BOND AT THE LEAD FRAME	KIRKENDALL VOIDING IN $AuAl_2$	EXCESSIVE $AuAl_2$ FORMATION DURING BONDING	0	2	3.1.4	C13
SURFACE INSTABILITY FAILURES								
5	HIGH V_{O3} (LOT A) LOW V_{OH3} (LOT B) HIGH I_{SS} [31] (7)	LOW V_{TH} AND HIGH I_{DSS}, Q4-Q5-Q6	CATION DRIFT I	CONTAMINATED GATE OXIDE	46 (4 FSS)	14	3.2.1	C14-C15
6	HIGH I_{SS} [31] (7)	HIGH I_{DSS}, Q4-Q5-Q6	CATION DRIFT II	CONTAMINATED GATE OXIDE	0	19	3.2.2	C16
7	LOW V_{OH2} (LOT A) LOW V_{OH1} (LOT B)	HIGH $V_{DS(ON)}$ DUE TO V_{TH} INCREASE IN Q1-Q2	INCREASE IN THE "FIXED" POSITIVE CHARGE DENSITY (SLOW HOLE TRAPPING)	GATE OXIDE DESIGN/ PROCESSING	8	18⚠	3.2.3	C17
8	I_{SS} (8)	DRAIN-SOURCE PUNCH-THROUGH, Q1-Q2 OR DEGRADED DRAIN, Q3	ION MIGRATION	MOBILE CONTAMINANT SURFACE IONS	0	6	3.2.4	C18
9	o I_{SS} (7) AND (8) o I_{IL} (34)	DEGRADED CR7-8/R3 AND P-WELL JUNCTIONS	ION MIGRATION	MOBILE CONTAMINANT IONS	0	1	3.2.4	C19
TEST ERROR								
10	OPEN PIN	EXTERNAL LEAD FOLDED UNDER	MECHANICAL OVER-STRESS	MISHANDLING	0	1	3.3.1	-
11	OPEN PINS	OPEN Al STRIPES	Al ELECTROMIGRATION	ELECTRICAL OVERSTRESS	0	1	3.3.1	C20
				TOTAL NUMBER OF FAILED PARTS	192 (4 FSS)	94		

NOTES

⚠ THESE 18 FAILURES WERE ALSO DUE, IN PART, TO THE CATEGORY 3 MECHANISM.
[ ] = TEST NO. FOR LOT A
( ) = TEST NO. FOR LOT B
FSS = FORMAL STEP STRESS
REFER TO TABLES 4 AND 6 FOR DISTRIBUTION OF FAILURES BY TIME, TEMPERATURE, AND VOLTAGE.

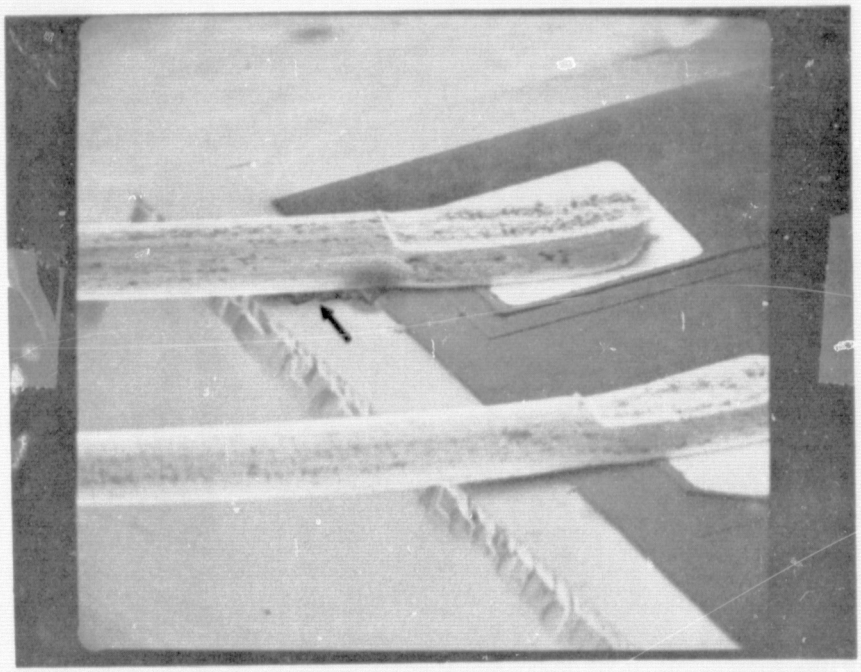
3.0 FAILURE ANALYSIS REPORTS

3.1 Mechanical and Bulk Failures

3.1.1 Wire-To-Die Short - 33 parts failed due to an internal short-circuit between one of the pins and pin 14 (V_{DD}). The value of the shorts ranged from 130 ohms to 5,000 ohms and the distribution of the shorts by pin number is shown in Table C2. In each case, the aluminum interconnect wire had shorted to the unpassivated edge of the substrate (V_{DD}) as illustrated in Figures C1 through C4. Each time an aluminum-silicon reaction had occurred at the point of contact as shown in Figures C2 and C4. The failures were attributed to a combination of the following design factors and workmanship errors:

1) The bonding pads are located relatively close to the edge of the die (see Figure C3).
2) The use of ultrasonically bonded wires in a low profile cavity resulted in wires departing the bonding pad at very shallow angles (see Figure C1). A relationship between the angle of departure and the incidence of failure is evident from Table C2. The Lot A package contains a rectangular cavity [see Appendix B1] and consequently, the longer corner wires which would have the shallowest angles (pins 1, 6, 7, 8, 9, and 13) failed first. The Lot B device has an almost square cavity [see Appendix B2] and equal wires lengths. Consequently, the failures were more randomly distributed.
3) The bonds were misplaced toward the edge of the die such that the heel of the bond was almost situated in the scribe area (see Figures C1 and C3).
4) Many of the failures contained a trail of smeared pad metal or entrapped debris beneath the wire that extended into the scribe area (see Figure C4).

The failure mechanisms involved sagging or flexing of the wire until contact was made (if the wire was not already touching) and then Al-Si alloying until sufficient ohmic contact was formed to cause a detectable short. Both mechanisms are essentially nonvoltage dependent.

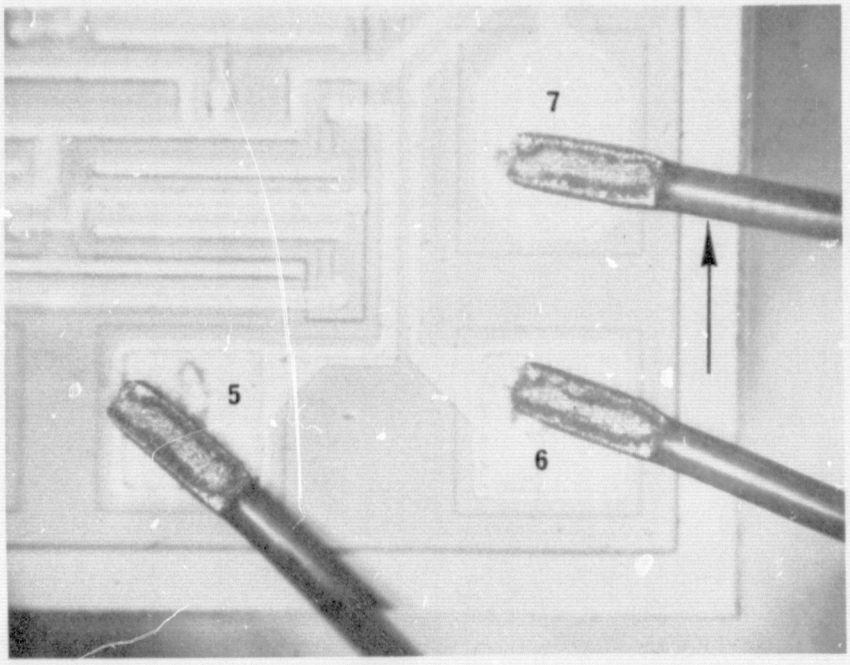


500X (SEM - 1.1 KV) S/N 105 - LOT A

FIGURE C1. EXAMPLE OF TYPICAL WIRE-TO-DIE SHORT (ARROW).

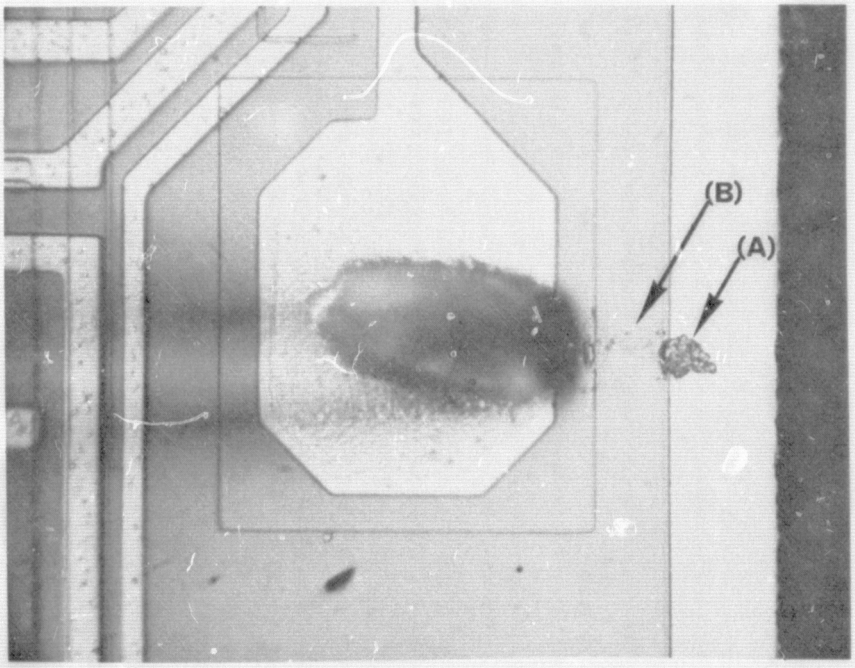
2250X (SEM - 1.1 KV) S/N 105 - LOT A

FIGURE C2. CLOSE-UP OF THE REACTION PRODUCT BETWEEN THE WIRE AND THE BARE SILICON.



200X S/N 273 - LOT A

FIGURE C3. VERTICAL VIEW OF A DEVICE WITH A PIN 7 TO DIE SHORT WHERE DENOTED BY THE ARROW.



400X S/N 273 - LOT A

FIGURE C4. PIN 7 SHORT SITE AFTER LIFTING ASIDE THE WIRE TO SHOW THE Al-Si REACTION PRODUCT (A) AND A TRAIL OF ALUMINUM DEBRIS (B).

TABLE C2. DISTRIBUTION OF THE PIN-TO-V_{DD} SHORTS

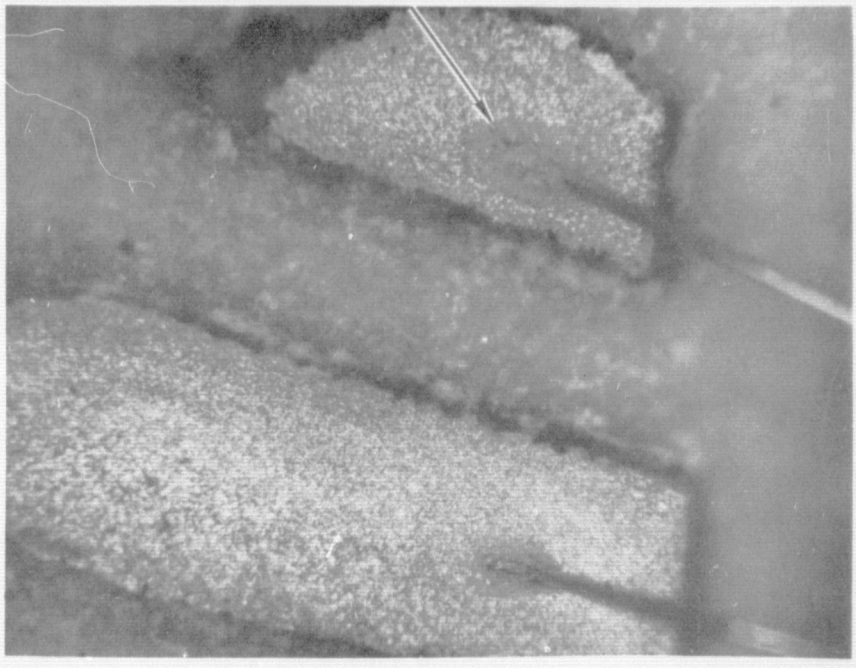
LOT A		LOT B	
PIN NO.	QUANTITY SHORTED TO V_{DD}	PIN NO.	QUANTITY SHORTED TO V_{DD}
6	6	1	4
7	9	3	2
9	1	4	4
13	1	6	1
	17	7	1
		8	3
		12	1
			16

3.1.2 Cracked Package - 121 Lot A parts developed gross leaks due to cracking of the glass seal which allowed moisture to enter the package. This resulted in the following three distinct types of failures with some parts exhibiting more than one failure mode:

1) 71 parts failed due to excessive pin-to-pin leakage currents. The leakages were traced to moisture that had condensed on the die (during cool-down) and created conductive paths between wires and bonding pads.
2) 16 parts failed due to an open pin. The failures were traced to open Al-Au wire bonds at the lead frame. Moisture had collected at the heel of the bond, as shown in Figure C5, and corroded open the aluminum wire at this point.
3) 62 parts failed due to excessive I_{DSS} and low threshold voltage in the n-channel transistors, Q4, Q5 and Q6. These failures were bake reversible. It is believed that at elevated temperature, water vapor diffused through imperfections in the passivation layers and injected a positive charge (such as H^+ or Na^+ ions) into the gate oxide. The cations drifted through the n-channel transistor gate oxide to the Si-SiO_2 interface resulting in reduced threshold voltage and increased I_{DSS}.

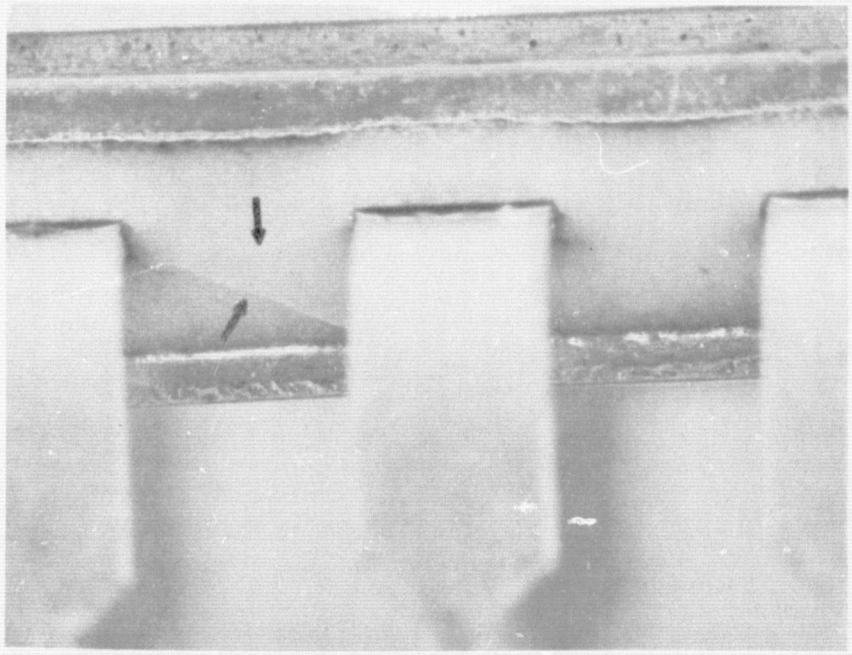
The failed devices exhibited gross leaks (fluorocarbon test) from cracks in the glass seal. The cracks always radiated from the Kovar leads as illustrated in Figure C6. The failures did not appear until after 256 hours of test, and appeared at every test point thereafter. This indicated that the cracks were the result of thermal expansions and contractions of the package and lead frame during insertion and removal of the test chassis from the high temperature test environment. Since each failure was the result of at least one mechanism (cracking) that is nonvoltage dependent, these 121 failures are not considered voltage dependent failures.

3.1.3 Excessive Ohmic Contact Resistance - These 16 Lot B parts failed due to excessive V_{OL2} and/or low V_{OH2}. Six parts failed V_{OL2} [24] (pins 13/8 inverter), two parts failed V_{OL2} [25] (pins 1/5 inverter), five parts failed V_{OH2} [12] (pins 13/8 inverter), and three parts failed both V_{OL2} [24] and V_{OH2} [12]. The failed values ranged from 600 mV to 639 mV for V_{OL2} and from 3.989 volts to



70X S/N 472 - LOT A

FIGURE C5. ACCUMULATION OF MOISTURE AND REACTION PRODUCTS (ARROW) AROUND AN OPEN WIRE BOND.



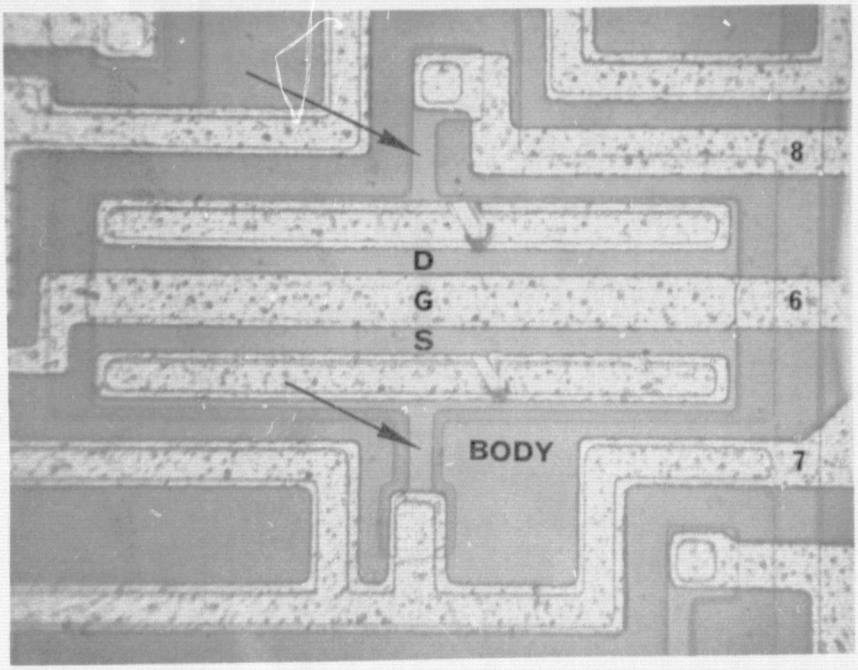
22X S/N 124 - LOT A

FIGURE C6. CRACKS IN THE GLASS SEAL RADIATING FROM THE KOVAR LEADS.

3.914 volts for V_{OH2} (1,011 mV to 1,086 mV in terms of p-channel transistor on-voltage). These failures would not recover upon baking (in fact the failed parameters usually worsened) which indicated that they were due to a bulk or mechanical mechanism.

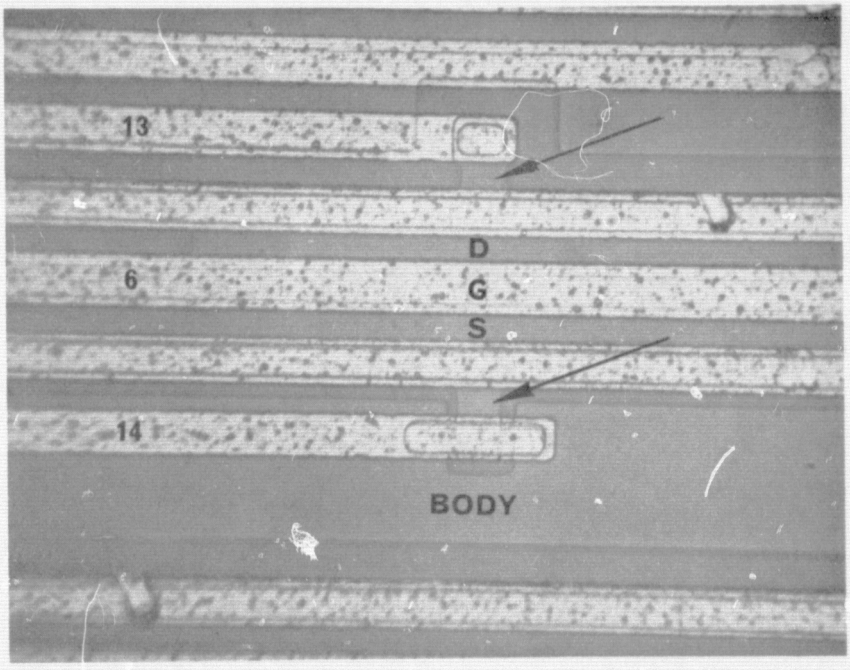
The failures were traced to excessive high-current on-voltage in n-channel transistors Q4 (nine parts) or Q5 (two parts), or in p-channel transistor Q1 (eight parts). Each transistor on the die contains a diffused resistor in series with its drain and its source (extensions of the drain and source diffusions) as illustrated in Figures C7 and C8. Consequently, the total transistor on-voltage is composed of the IR drops across these resistors and the actual channel on-voltage. Die level probing disclosed that the drop across the series source resistor (R_S) of the failed transistors was excessive as illustrated in Table C3. This results in an increase in the total transistor on-voltage, not only due to added series IR drop, but also because this added drop reduces the gate to source voltage which in turn increases the channel on-voltage.

Because it was not likely that the bulk resistance of R_S could have increased during accelerated life, it was suspected that the excessive drop was caused by degradation of the ohmic contact. However, the drop across the source ohmic contacts of Q1 and Q4 could not be determined because their source resistors are shorted to the body diffusions via enlarged contact windows as can be seen in Figure C7 and C8. Proof of ohmic contact deterioration was obtained by leaving some of the failed parts on test through 4,000 hours. This resulted in degradation of other measurable contacts. For example, S/N 135 which had originally failed only V_{OH2} [12] (Q1) at 32 hours in Cell 102 was left on test through 4,000 hours. As shown in Table C4, both the drain and the source resistors of all of the transistors eventually displayed excessive drops. The ohmic contacts of the source resistors of Q2, Q3, Q5 and Q6 and all of the drain resistors could be evaluated by examing the forward body to source or drain I-V characteristics. Figure C9 shows forward diode curves of the source and drain junctions of Q3 compared to that of a normal unstressed Q3 source junction. Figure C10 shows forward curve curves of the drain junction of Q6 and of the source junction of Q5 compared to that of a normal, unstressed Q5 source junction.



490X S/N 215 - LOT B

FIGURE C7. Q4 SHOWING THE LOCATION OF THE SERIES DRAIN AND SOURCE RESISTORS (ARROWS).



490X S/N 215 - LOT B

FIGURE C8. Q1 SHOWING THE LOCATION OF THE SERIES DRAIN AND SOURCE RESISTORS (ARROWS).

TABLE C3. RESULTS OF ANALYSIS OF S/N 215 WHICH FAILED V_{OL2} [24] AND V_{OH2} [12] AFTER 128 HOURS IN CELL 301.

I. PARAMETER HISTORY			
	PRESTRESS VALUE	AT 128 HOURS	POST BAKE VALUE
V_{OL2} [24] (Q4)	.473 V	.603 V	.600 V
V_{OH2} [12] (Q1)	4.159 V	3.914 V	3.900 V

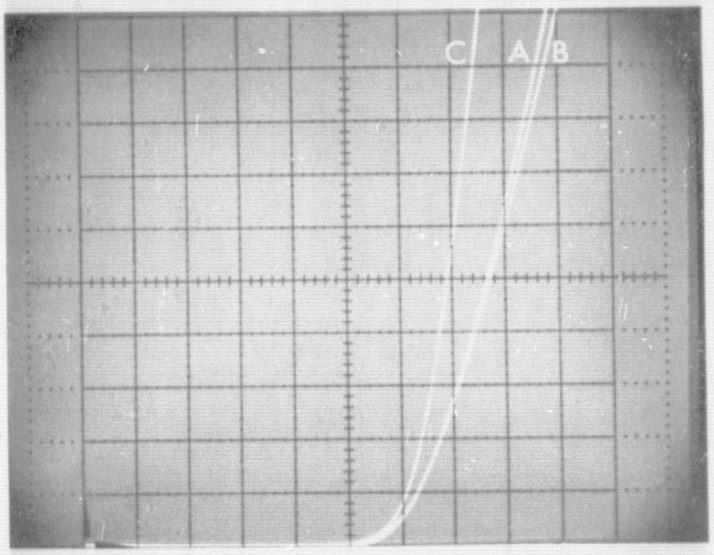
II. RESULTS OF DIE LEVEL PROBING				
		TOTAL ON-VOLTAGE	DROP ACROSS R_{DRAIN}*	DROP ACROSS R_{SOURCE}*
A. S/N 215	Q4	602 mV	42 mV	132 mV
	Q5	472 mV	43 mV	51 mV
	Q6	459 mV	55 mV	46 mV
	Q1	1104 mV	113 mV	382 mV
	Q2	740 mV	106 mV	134 mV
	Q3	792 mV	150 mV	154 mV
B. UNSTRESSED SAMPLE (S/N 455) FOR COMPARISON	Q4	397 mV	36 mV	52 mV
	Q5	377 mV	39 mV	38 mV
	Q6	377 mV	50 mV	40 mV
	Q1	650 mV	50 mV	53 mV
	Q2	700 mV	53 mV	55 mV
	Q3	660 mV	57 mV	55 mV

* MEASURED DURING THE V_{OH2} OR V_{OL2} TEST (I_{DS} = -750 µA OR 600 µA).

TABLE C4. RESULTS OF ANALYSIS OF S/N 135 AFTER 4000 HRS OF STRESS IN CELL 102

I. PARAMETER HISTORY			
	PRESTRESS VALUE	AT 32 HOURS	AT 4000 HOURS
V_{OH2} [12] (Q1)	4.027 V	3.953 V	3.213 V
V_{OH2} [13] (Q2)	4.281 V	4.234 V	3.928 V
V_{OH2} [14] (Q3)	4.319 V	4.310 V	4.144 V
V_{OL2} [24] (Q4)	.410 V	.439 V	19 V
V_{OL2} [25] (Q5)	.400 V	.422 V	17 V
V_{OL2} [26] (Q6)	.404 V	.410 V	.898 V

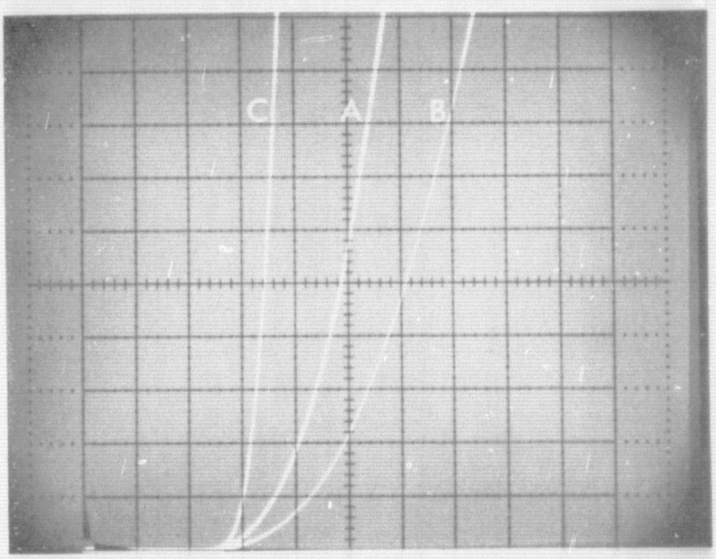
II. RESULTS OF DIE LEVEL PROBING			
TRANSISTOR	TOTAL ON-VOLTAGE	DROP ACROSS R_{DRAIN}	DROP ACROSS R_{SOURCE}
Q1	1,660 mV	102 mV	505 mV
Q2	940 mV	168 mV	169 mV
Q3	850 mV	171 mV	177 mV
Q4	19,360 mV	130 mV	640 mV
Q5	17,540 mV	140 mV	610 mV
Q6	895 mV	412 mV	130 mV



HORIZONTAL = 100mV/DIV
VERTICAL = 100μA/DIV

S/N 135 - LOT B

FIGURE C9. FORWARD DIODE CURVES OF THE DRAIN JUNCTION (A) AND THE SOURCE JUNCTION (B) OF Q3 OF S/N 135 COMPARED TO THE Q3 SOURCE JUNCTION (C) OF AN UNSTRESSED PART.



HORIZONTAL = 200mV/DIV
VERTICAL = 100μA/DIV

S/N 135 - LOT B

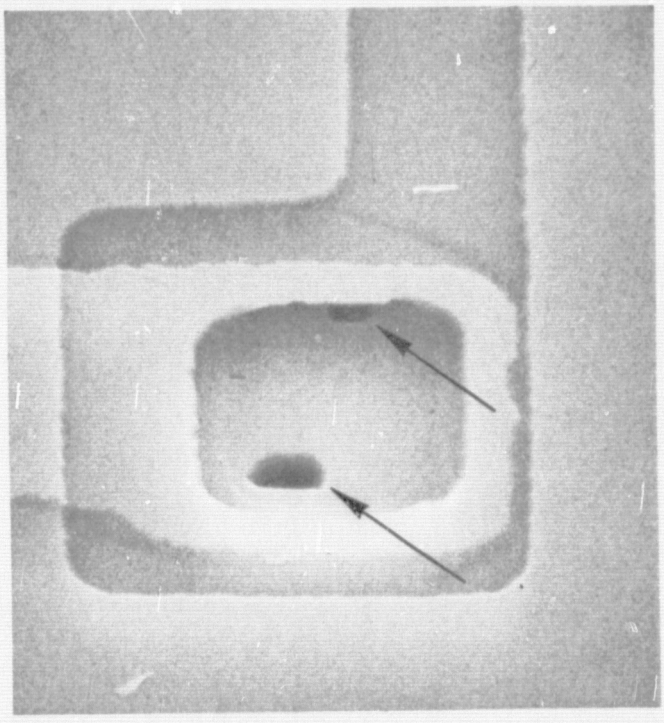
FIGURE C10. FORWARD DIODE CURVES OF THE Q6 DRAIN JUNCTION (A) AND THE Q5 SOURCE JUNCTION (B) OF S/N 135 COMPARED TO THE Q5 SOURCE JUNCTION (C) OF AN UNSTRESSED PART.

In each instance the forward curve through the suspect contact contained an added resistive component. The drop across this added component was equal to the amount of excess drop measured across the resistor. This provided evidence that the V_{OL2} and the V_{OH2} failures were due to degradation of the source ohmic contact.

Based on die level probing, SEM examinations, and consideration of the contact geometry, metallization step coverage problems (discontinuities, etc.) were eliminated as the cause of the contact deterioration. SEM examinations of defective contacts after etching away the aluminum disclosed that all contained deep etch pits in the silicon as illustrated in Figures C11 and C12. This indicated that a large amount of silicon from these areas had dissolved into the aluminum. Dissolved silicon would tend to precipitate out at the aluminum grain boundaries causing loss of cohesion and thus, increased resistivity. The fact that the source ohmic contacts of Q1 and Q4 exhibited the earliest degradation further indicates that the mechanism involved silicon dissolution. Due to the enlarged source contact windows of Q1 and Q4 more silicon is available to dissolve and enter the stripe at these two contacts than at any other contact. The problem was caused by a manufacturing anomaly (probably involving the metallization alloy cycle) as indicated by the fact that, upon receipt, a high percentage of the Lot B parts did not meet the M38510 specification limits for V_{OL2} and V_{OH2}.

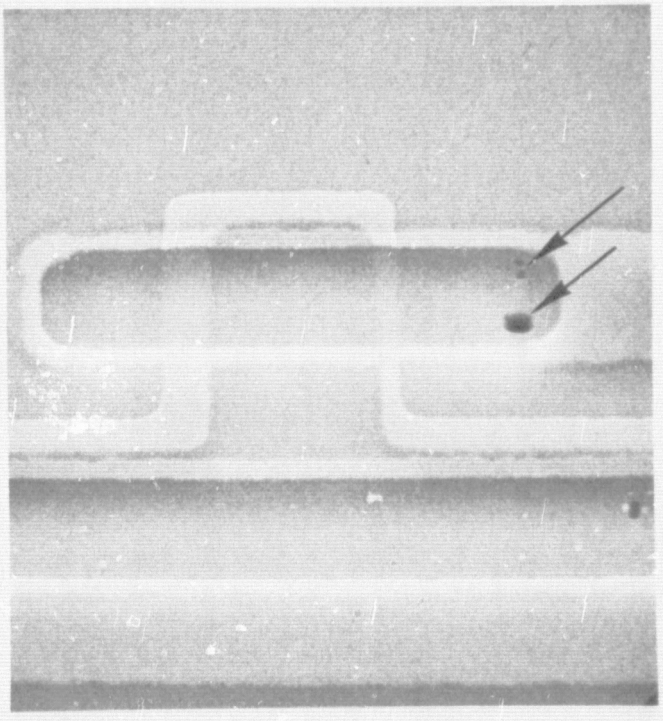
These particular failures did not depend on the applied voltage, as indicated by the fact that the degradation progressed at the same rate during unpowered bakes. Thus, these 16 failures are not considered voltage dependent failures.

3.1.4 Lifted Bond - Two Lot B parts failed due to an open pin. The open pin was traced to a lifted Al-Au wire bond at the lead frame. Examination of the underside of the bonds disclosed that they had fractured through an intermetallic zone as shown in Figure C13. This suggested that the open was caused by Kirkendahl voiding. The intermetallics were purple colored indicating that the voiding had occurred in $AuAl_2$. These two failures occurred at 1,000 and 2,000 hours of accelerated life. Since no other parts exhibited this mechanism after 2,000



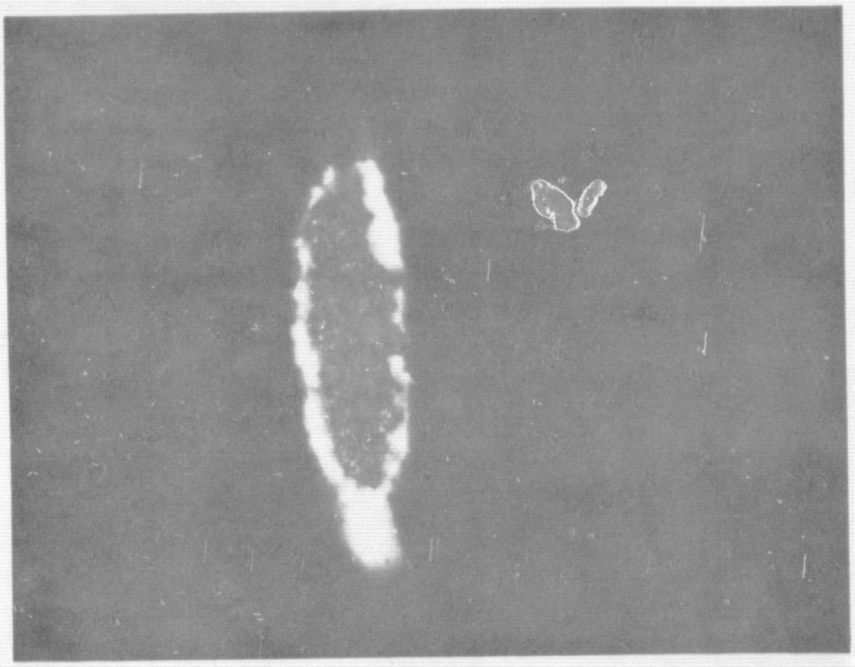
3000X (SEM - 25 KV) S/N 135 - LOT B

FIGURE C11. ALLOY PITS IN Q5 SOURCE OHMIC CONTACT REVEALED BY ALUMINUM ETCH.



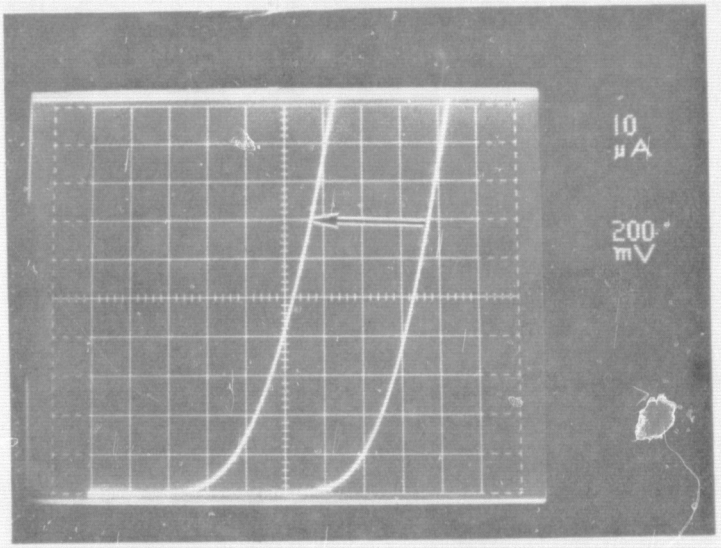
2000X (SEM - 25 KV) S/N 135 - LOT B

FIGURE C12. ALLOY PITS IN Q1 SOURCE OHMIC CONTACT REVEALED BY ALUMINUM ETCH.



395X S/N 412 - LOT B

FIGURE C13. UNDERSIDE OF THE LIFTED BOND SHOWING INTERMETALLICS.



S/N 411 - LOT B

FIGURE C14. EXAMPLE OF THE THRESHOLD VOLTAGE SHIFT THAT OCCURRED IN Q6 OF A V_{OH3} FAILURE. LEFT HAND TRACE IS THAT OF A FAILED Q6; RIGHT HAND TRACE IS THAT OF A NORMAL TRANSISTOR. V_{TH} CHARACTERISTIC = I_{DS} VS. V_{DS}, $V_{GS} = V_{DS}$

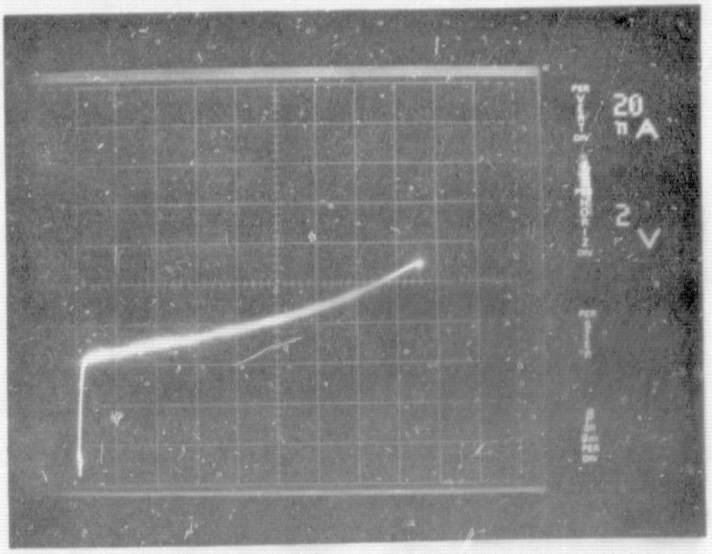
additional hours of testing, the two opens were attributed to excessive $AuAl_2$ formation during the bonding operation.

3.2 Surface Instability Failures

3.2.1 Cation Drift I - 46 Lot A parts failed due to excessive no-load, output high, p-channel transistor on-voltage (V_{O3}); 33 failed V_{O3} [21] (pin 12 inverter), 6 failed V_{O3} [20] (pins 1/5 inverter), 5 failed V_{O3} [19] (pins 13/8 inverter), and 2 failed both V_{O3} [20] and V_{O3} [19]. 21 of these parts also failed due to excessive quiescent supply current, outputs high (I_{SS} [31]). The failed values ranged from 11 mV to 506 mV for V_{O3} and from 63 nA to greater than 1.8 μA (established upper test limit) for I_{SS} [31]. All failures occurred within 16 hours and were bake reversible.

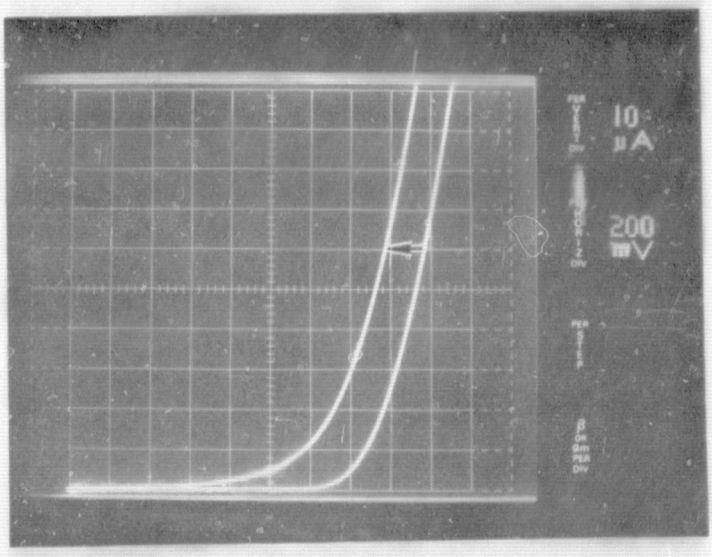
14 Lot B parts failed due to low no-load, high-level output voltage (V_{OH3}); 13 failed V_{OH3} [17] (pin 12 inverter) and one failed V_{OH3} [15] (pins 13/8 inverter). Seven of these parts also failed due to excessive I_{SS} [7]. The failed values ranged from 4.949 volts to 4.684 volts for V_{OH3} (51 mV to 316 mV in terms of p-channel transistor on-voltage) and from 54 nA to 1.8 μA for I_{SS} [7]. All but one of these failures occurred within one hour and all were bake reversible.

The failures were traced to low threshold voltage (V_{TH}) and high cutoff current (I_{DSS}) in an n-channel transistor (Q4, Q5 or Q6). V_{OH3} (or V_{O3}) failure was caused by a V_{TH} shift like that shown in Figure C14. Due to the low V_{TH}, the transistor Q6 drew about 60 μA (should be 0 μA) during the V_{OH3} [17] test (V_{GS} = +1.1V) through the complementary p-channel transistor Q3. As a result, the on-voltage of Q3 is forced to exceed the specified limit of 50 mV ($5V-V_{OH3}$). The I_{SS} failure was caused by excessive cutoff current, I_{DSS}, that accompanied the low V_{TH} in some instances. I_{DSS} always saturated as illustrated in Figure C15 and the drain and source junctions displayed no degradation indicating that the high I_{DSS} was the result of current flow through an inversion layer across the channel region. These 60 failures are summarized in terms of the degraded transistor and its failure mode in Table C5.



S/N 222 - LOT B

FIGURE C15. I_{DSS} VS. V_{DS} (V_{GS} = 0 V) OF Q6 OF AN I_{SS} [7] FAILURE.



S/N 222 - LOT B

FIGURE C16. EXAMPLE OF THE SHIFT IN THE V_{TH} CHARACTERISTIC THAT OCCURRED IN Q6 OF AN I_{DSS} FAILURE (I_{DSS} = 100 nA). L/H TRACE IS THAT OF A FAILED Q6, R/H TRACE IS THAT OF A NORMAL TRANSISTOR. V_{TH} CHARACTERISTIC = I_{DS} VS V_{DS}, V_{GS} = V_{DS}.

C.2

TABLE C5. DISTRIBUTION OF V_{OH3} (V_{O3}) AND I_{SS} FAILURES BY DEGRADED TRANSISTOR AND FAILURE MODE

DEGRADED TRANSISTOR	QUANTITY WITH ONLY LOW V_{TH}	QUANTITY WITH BOTH LOW V_{TH} AND HIGH I_{DSS}	TOTAL
LOT A			
Q6	19	14	33
Q5	3	3	6
Q4	2	3	5
Both Q5 and Q4	1	1	2
LOT B			
Q6	6	7	13
Q5	0	0	0
Q4	1	0	1

The failure modes and the bake recovery displayed by these parts indicate that the V_{TH} decrease and the I_{DSS} increase were caused by the accumulation of a net positive charge in the gate oxide at the Si/SiO_2 interface. In the case of Q6, the accumulation would have resulted from inward drift of mobile cation surface contamination, such as Na^+ ions, through the gate oxide under the influence of the +15 volt gate bias. In the case of Q4 or Q5, the accumulation probably resulted from lateral drift of cations into the gate oxide due to the 15 volt reverse bias on the drain junction. The accumulated charge lowered the threshold voltage to the point that V_{OH3} (or V_{O3}) failed and, in the more severe cases, inverted the channel region causing excessive I_{DSS}.

3.2.2 Cation Drift II - 19 Lot B parts failed due to excessive quiescent supply current, outputs high (I_{SS} [7]). The failures occurred between 1 and 2,000 hours and were bake reversible. The high I_{SS} was traced to excessive I_{DSS} in n-channel transistors Q4 or Q6. Seventeen parts failed due to high Q6 I_{DSS} and two parts failed due to high Q4 I_{DSS}. As was the case with the cation Drift I type failures, I_{DSS} of these parts always saturated (same as Figure C15) and the drain and source junctions displayed no degradation. Thus, these failures were similarly attributed to a cation drift mechanism. However, these 19 failures were segregated from those identified as type I drift for two reasons:

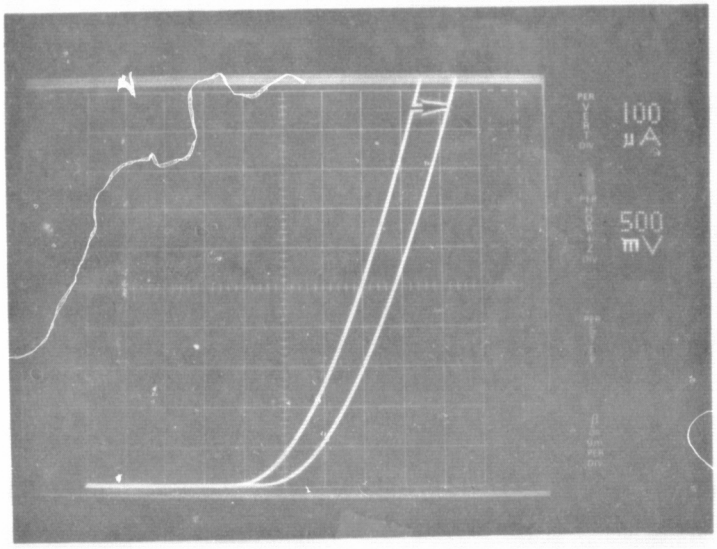
1) I_{SS} failure was not accompanies by V_{OH3} failure. The transistors which exhibited high I_{DSS} showed decreased V_{TH}, as illustrated in Figure 16, but the V_{TH} shift was not severe enough to cause V_{OH3} failure. In the case of evenly distributed positive charge at the gate oxide/Si interface, the quantity of charge required to cause I_{DSS} failure is slightly greater than that required to cause V_{OH3} failure. In other words, I_{DSS} failure always should have been accompanied by V_{OH3} as was the case with type I drift. Analysis of these 19 parts established that the anomalous current was confined to the active channel region itself; i.e., it was not the result of a shunt or parasitic inversion path beneath the field oxide. Consequently, it is believed that, in the case of the type II drift, the cation contamination may have been either non-uniformly distributed initially or drifted non-uniformly.

2) These 19 failures were distributed between 1 and 2,000 hours, whereas all but one of the Lot B type I failures occurred within one hour. Apparently, either the level of contamination was significantly lower in the case of type II failure than in type I, or a different, less mobile species of charge was responsible for the type II failures.

3.2.3 Slow Trapping - Eight Lot A parts failed V_{OH1} [13 and/or 14] and eighteen Lot B parts failed V_{OH2} [12 and/or 13] due to a bake reversible mechanism. The failed values ranged from 3.598 to 3.406 volts for V_{OH1} (1,402 mV to 1,594 mV in terms of p-channel on-voltage) and from 3.997 volts to 3.875 volts for V_{OH2} (1,003 mV to 1,125 mV in terms of p-channel on-voltage). The 18 Lot B failures occurred between 128 and 4,000 hours. The Lot A failures also began to appear at 128 hours, but the distribution was truncated at 256 hours by the cracked seal problem.

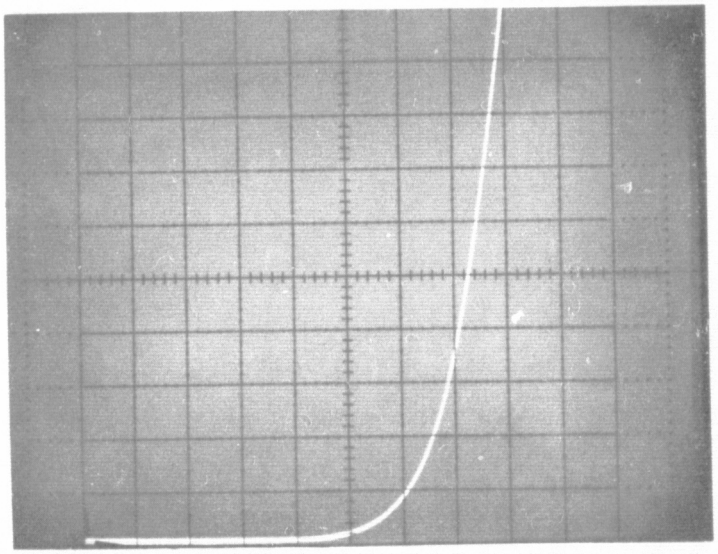
The V_{OH} failures were traced to excessive on-voltage in p-channel transistors Q1 and Q2 primarily caused by an increase in threshold voltage as illustrated in Figure C17. Negative bias ($-V_{DD}$) had been applied to the gates of Q1 and Q2 during accelerated life. P-channel V_{TH} increase under negative gate bias indicates that the shift was caused by an increase in the "fixed" positive surface charge density. This is generally attributed to a slow hole trapping mechanism. In the case of the Lot B failures, the V_{OH2} of the eighteen category 7 failures would return to within specification after baking but would not completely recover to the pre-stress value. V_{OH2} would saturate at 110 to 120% of the pre-stress value after extended baking. Die level probing established that the resistance of the ohmic contacts of Q1 and Q2 had increased. However, since these failures were predominately due to V_{TH} shift, they are categorized as voltage dependent surface instability type failures.

3.2.4 Miscellaneous Surface Instability Failures - Six Lot B parts failed quiescent supply current, outputs low (I_{SS} [8]) due to excessive I_{DSS} in a p-channel transistor (Q1, Q2 or Q3). The failed I_{SS} [8] values ranged from 74 nA to 541 nA and were bake reversible. Three parts failed due to excessive Q3 I_{DSS}, two parts due to excessive Q2 I_{DSS}, and one part due to excessive Q1 I_{DSS}. The



S/N 21 - LOT A

FIGURE C17. EXAMPLE OF THE THRESHOLD VOLTAGE SHIFT THAT OCCURRED IN Q2 UNDER NEGATIVE GATE BIAS. L/H TRACE IS THE V_{TH} CHARACTERISTIC OF A NORMAL TRANSISTOR. R/H TRACE IS THAT OF THE FAILED Q2. V_{TH} CHARACTERISTIC = I_{DS} VS. V_{DS}, $V_{GS} = V_{DS}$.



HORIZONTAL = 2 VOLTS/DIVISION
VERTICAL = 10 nA/DIVISION

S/N 141 - LOT B

FIGURE C18. I_{DSS} VS. V_{DS} OF Q2 OF AN $I_{SS[8]}$ FAILURE.
($I_{SS[8]}$ = 65 nA AT 15 VOLTS)

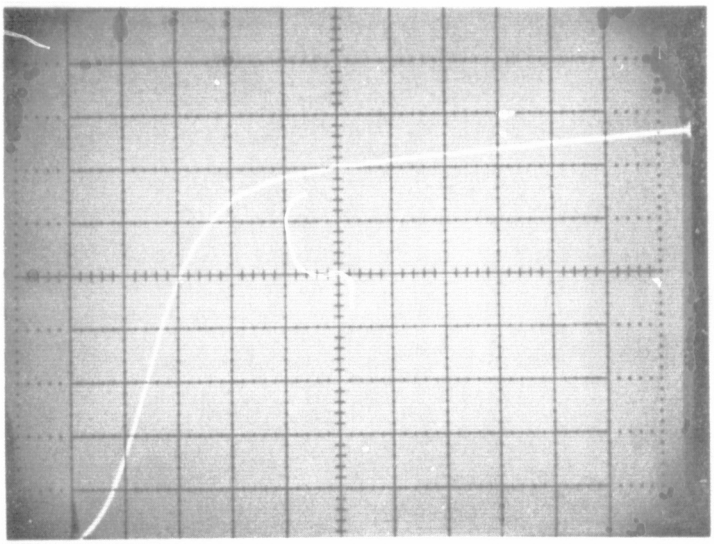
degraded Q1 and Q2 transistors displayed exponentially increasing leakage current above a drain-source potential of about 10 volts as illustrated in Figure C18. The drain and source junctions displayed no degradation and the anomalous current could be pinched off by applying a positive gate to source bias. This indicated that the excessive I_{DSS} was the result of drain-source punch-through. The degraded Q3 transistors displayed an I_{DSS} characteristic essentially like that of the Q1 and Q2 transistors, but in the case of Q3 the excessive leakage was traced to a degraded drain junction. It was found that some of failed parts would recover immediately upon delidding or upon removal of the glassivation (the other parts had been cured by baking before delidding). This indicated that the degradation was caused by mobile surface ions and that the failure mechanism involved charge migration.

One Lot B part failed I_{SS} [7] (72 nA), I_{SS} [8] (81 nA) and I_{IL} [34] (37 nA). The I_{SS} failures were caused by a degraded p-well junction and the I_{IL} failure was caused by a degraded input protection network between V_{DD} and pin 10 (CR7-8 and R3). The degraded junctions displayed channelled characteristics, as illustrated in Figure C19, which recovered when baked. Consequently, the degradation was attributed to mobile contaminant ions which migrated during accelerated life.

3.3 Miscellaneous Failures

3.3.1 Test Error - One Lot B part was removed from test because it exhibited an open-circuit at pin 6. It was subsequently discovered that pin 6 had been accidentally folded under the package during insertion into the test socket.

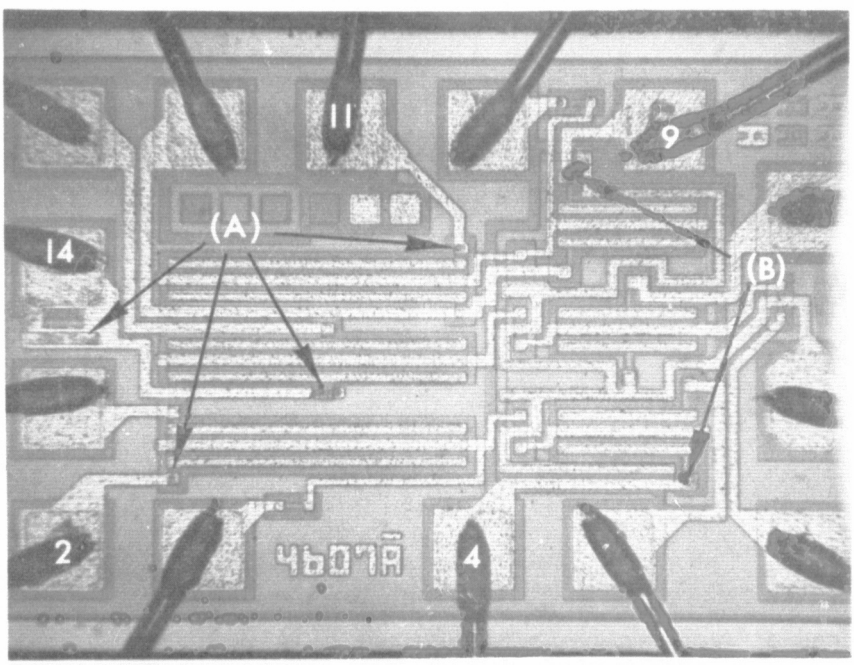
One Lot B part failed due to open and resistive pins after 2,000 hours in cell 101. Several metallization stripes were open or depleted at the ohmic contact. Depleted metal was found at the p-channel source contacts and whisker growth was found at the n-channel source contacts as shown in Figure C20. This indicated that the failures were the result of aluminum electromigration due to excessive current from V_{DD} to V_{SS} through each inverter. The part contained no deficiency which would explain a high current condition. Therefore, this isolated failure was attributed to a random test error.



HORIZONTAL = 2 VOLTS/DIVISION
VERTICAL = 10 nA/DIVISION

S/N 425 - LOT B

FIGURE C19. REVERSE CHARACTERISTIC OF THE DEGRADED P-WELL JUNCTION.



105X

S/N 362 - LOT B

FIGURE C20. DIE SURFACE SHOWING DEPLETED ALUMINUM (A) AND WHISKER GROWTH (B) AT OHMIC CONTACTS.